SVR ENGINEERING COLLEGE

Approved by AICTE & Permanently Affiliated to JNTUA

Ayyalurmetta, Nandyal – 518503. Website: www.svrec.ac.in

Department of Electronics and Communication Engineering

(20A04403P) LINEAR & DIGITAL IC APPLICATIONS LABORATORY R20

II B. Tech (ECE) II Semester 2021-22

STUDENT NAME	
ROLL NUMBER	
SECTION	

SVR ENGINEERING COLLEGE

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DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

ACADEMIC YEAR: 2021-22

This is to certify that the bonafide record work done by

*Mr./Ms.*____*bearing*

*H.T.NO.*_____________________ *of II B. Tech II Semester in the*

LINEAR AND DIGITAL IC APPLICATIONS LABORATORY.

Faculty In-Charge **Head of the Department**

LAB SYLLABUS COPY

20A04403P	LINEAR AND DIGITAL IC APPLICATIONS LAB		0	0	3	1.5
Pre-requisite	Analog Circuits Lab, Digital Logic Design Lab	**Semester**	**IV**			

Course Objectives:

The objective of the course is to learn design, testing and characterizing of circuit behaviour with digital and analog ICs.

Course Outcomes (CO):

CO1: Understand the pin configuration of each linear/ digital IC and its functional diagram.
CO2: Conduct the experiment and obtain the expected results.
CO3: Analyze the given circuit/designed circuit and verify the practical observations with the analyzed results.
CO4: Design the circuits for the given specifications using linear and digital ICs.
CO5: Acquaintance with lab equipment about the operation and its use.

List of Experiments:

PART – I: Linear IC Experiments

1. OP AMP Applications – Adder, Subtractor, Comparators.
2. Integrator and Differentiator Circuits using IC 741.
3. Active Filter Applications – LPF, HPF (first order)
4. IC 741 Waveform Generators – Sine, Square wave and Triangular waves.
5. IC 555 Timer – Monostable and Astable Multivibrator Circuits.
6. Schmitt Trigger Circuits – using IC 741
7. IC 565 – PLL Applications.
8. Voltage Regulator using IC 723, Three Terminal Voltage Regulators – 7805, 7809, 7912.

PART – II: Digital IC Applications

1. 3-8 decoder using 74138
2. 4-bit comparator using 7485.
3. 8*1 Multiplexer using 74151 and 2*4 Demultiplexer using 74155.
4. D, JK Flip Flops using 7474, 7483.
5. Decade counter using 7490.
6. UP/DOWN counter using 74163
7. Universal shift registers using 74194/195.
8. RAM (16*4) using 74189 (Read and Write operations).

Note: At least 12 experiments shall be performed.

ECE DEPT VISION & MISSION PEOs and PSOs

Vision

To produce highly skilled, creative and competitive Electronics and Communication Engineers to meet the emerging needs of the society.

Mission

- Impart core knowledge and necessary skills in Electronics and Communication Engineering Through innovative teaching and learning.
- Inculcate critical thinking, ethics, lifelong learning and creativity needed for industry and society
- Cultivate the students with all-round competencies, for career, higher education and self-employability

I. PROGRAMME EDUCATIONAL OBJECTIVES (PEOS)

PEO1: Graduates apply their knowledge of mathematics and science to identify, analyze and solve problemsin the field of Electronics and develop sophisticated communication systems.

PEO2: Graduates embody a commitment to professional ethics, diversity and social awareness in theirprofessional career.

PEO3: Graduates exhibit a desire for life-long learning through technical training and professional activities.

II. PROGRAM SPECIFIC OUTCOMES (PSOS)

PSO1: Apply the fundamental concepts of electronics and communication engineering to design a variety of components and systems for applications including signal processing, image processing, communication, networking, embedded systems, VLSI and control system

PSO2: Select and apply cutting-edge engineering hardware and software tools to solve complex Electronics and Communication Engineering problems.

III. PROGRAMME OUTCOMES (PO'S)

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

IV. COURSE OBJECTIVES:

- T The objective of the course is to learn design of circuit behavior with analog ICs.
- The objective of the course is to learn testing of circuit behavior with analog ICs.
- The objective of the course is to learn characterizing of circuit behavior with analog ICs.
- The objective of the course is to learn design of circuit behavior with digital ICs.
- The objective of the course is to learn testing of circuit behavior with digital ICs
- The objective of the course is to learn characterizing of circuit behavior with digital ICs.

V. COURSE OUTCOMES:

After the completion of the course students will be able to

Course Outcomes	Course Outcome statements	BTL
CO1	Understand the pin configuration of each linear/ digital IC and its functional diagram.	L1
CO2	Conduct the experiment and obtain the expected results.	L2
CO3	Analyze the given circuit/designed circuit and verify the practical observations with the analyzed results.	L3
CO4	Design the circuits for the given specifications using linear and digital ICs	L4
CO5	Acquaintance with lab equipment about the operation and its use.	L5

VI. COURSE MAPPING WITH PO'S AND PEO'S:

Course Title	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
Linear & Digital IC Applications Lab	2.6	2.8	2.4	2.3	2.8	2.2	1.6	1.8	2.0	2.3	2.3	2.8	2.4	2.5

VII. MAPPING OF COURSE OUTCOMES WITH PEO'S AND PO'S:

Course Title	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1	3	3	3	2	3	2	3	1	3	3	3	3	3	3
CO2	2		3	2	2	2	1	2	1		3		2	3
CO3	2	3	2	2		3	2		2	1	1	3	2	2
CO4	3	2	2		3	2	1	2	2	2		2	2	
CO5	3	3	2	3	3	2	1	2	2	3	2	3	3	2

LABORATORY INSTRUCTIONS

1. While entering the Laboratory, the students should follow the dress code. (Wear shoes and White apron, Female Students should tie their hair back).

2. The students should bring their observation book, record, calculator, necessary stationery items and graph sheets if any for the lab classes without which the students will not be allowed for doing the experiment.

3. All the Equipment and components should be handled with utmost care. Any breakage or damage will be charged.

4. If any damage or breakage is noticed, it should be reported to the concerned in charge immediately.

5. The theoretical calculations and the updated register values should be noted down in the observation book and should be corrected by the lab in-charge on the same day of the laboratorysession.

6. Each experiment should be written in the record note book only after getting signature from the lab in-charge in the observation notebook.

7. Record book must be submitted in the successive lab session after completion of experiment.

8. 100% attendance should be maintained for the laboratory classes.

Precautions.

1. Check the connections before giving the supply.
2. Observations should be done carefully

I N D E X

Max. Marks per each experiment :5

Off the Syllabus :

PART – I: Linear IC Experiments

Sl. No.	Name of the Experiment	Page No.	Date of Performed	Date of Submission	Marks Obtained	Signature of lab in charge
1	OP AMP Applications – Adder, Subtractor, Comparators.	3-12				
2	Integrator and Differentiator Circuits using IC 741.	13-19				
3	Active Filter Applications – LPF, HPF (first order)	20-26				
4	IC 741 Waveform Generators – Sine, Square wave and Triangularwaves.	27-32				
5	IC 555 Timer – Mono stable andAstable Multivibrator Circuits.	33-41				
6	Schmitt Trigger Circuits – using IC 741	42-44				
7	IC 565 – PLL Applications.	45-49				
8	Voltage Regulator using IC 723, Three Terminal Voltage Regulators – 7805, 7809, 7912.	50-60				

PART – II: Digital IC Applications

Sl. No.	Name of the Experiment	Page No.	Date of Performed	Date of Submission	Marks Obtained	Signature of lab in charge
------	PART – B (Using Hardware) :	------				
01	3-8 decoder using 74138					
02	4-bit comparator using 7485					
03	8*1 Multiplexer using 74151 and 2*4 Demultiplexer using 74155.					
04	D, JK Flip Flops using 7474, 7483.					

PART – III **Beyond the Syllabus :**						
1	**Applications of Op-amp** **Design and test the performance of the following circuits using Op-amp IC741** **Inverting amplifier**					
2	**Precision rectifiers** **Conduct experiments on half wave and full wave precision rectifiers and draw the output wave forms.**					

PART – I

Linear IC Experiments

(Off the Syllabus)

Experiment No: 1 **Date:**

OP AMP Applications – Adder, Subtractor, Comparators.

AIM:

To design and study the op-amp as Adder (or) Summing amplifier

APPARATUS REQUIRED:

S. No.	Name of the Apparatus	Range	Quantity
1	Function Generator	3 MHz	1
2	CRO	30 MHz	1
3	Dual Regulated Power Supply	0-30V	1
4	CRO probes	--------	2

COMPONENTS REQUIRED:

S. No.	Name of the Apparatus	Quantity
1	Resistors 1kohm	4
2	IC-741	1
3	Bread board	1
4	Connecting wires	As required

LAB SPECIFICATIONS TAKEN:

Summer circuit design has been implemented on the virtual breadboard using following specifications:

- Power Supply: +12v and -12v
- Function generator: Selected wave with following specifications:

Frequency:1kHz
Amplitude: 2V
Duty cycle = 50%

THEORY:

Adder (or) Summing Amplifier: This is one of the liner applications of the Op-Amp. A circuit whose output is the sum of several input signals is called a summer. Shown in fig. is an inverting summer.

Theoretical Calculations:

$$V_o = -\left(\frac{Rf}{R1}V1 + \frac{Rf}{R2}V2 + \frac{Rf}{R3}V3\right)$$

EXAMPLE:

$$v_0 = -\left(\frac{2k\Omega}{2k\Omega} \times 2V + \frac{2k\Omega}{2k\Omega} \times 2V + \frac{2k\Omega}{2k\Omega} \times 2V\right)$$
$$\Rightarrow v_0 = -(2V + 2V + 2V)$$
$$\Rightarrow v_0 = -6V$$

PRACTICAL VALUES:

S. No.	V_1 (V)	V_2 (V)	Theoretical values(V_1+V_2)	Practical Values(V)
1	1	1	2	2.6
2	1	2	3	3.8
3	2	3	5	5.4

CIRCUIT DIAGRAM:

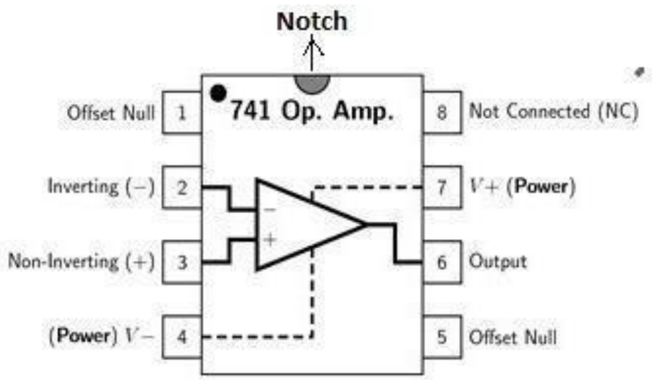


FIG: PIN DIAGRAM OF IC -741

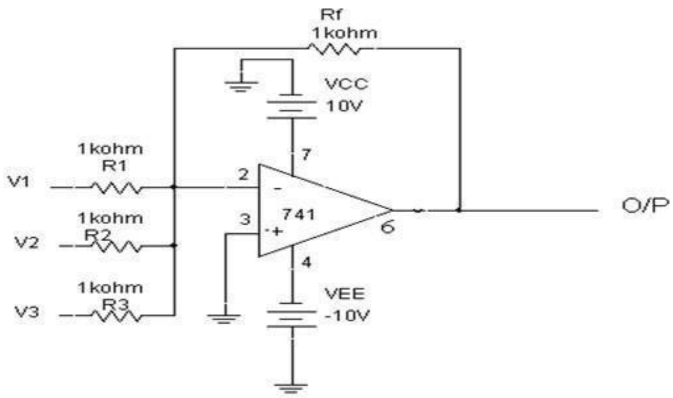


Fig: Adder(Inverting Summing Amplifier)

PROCEDURE:

1) Connect the circuit as per the given circuit diagram.
2) Apply biasing voltage at pins 4 and 7 as -10V and +10V respectively..
3) Observe the output at the pin no.6 with digital multimeter
4) Compare the theoretical and practical values.

EXPECTED WAVE FORMS:

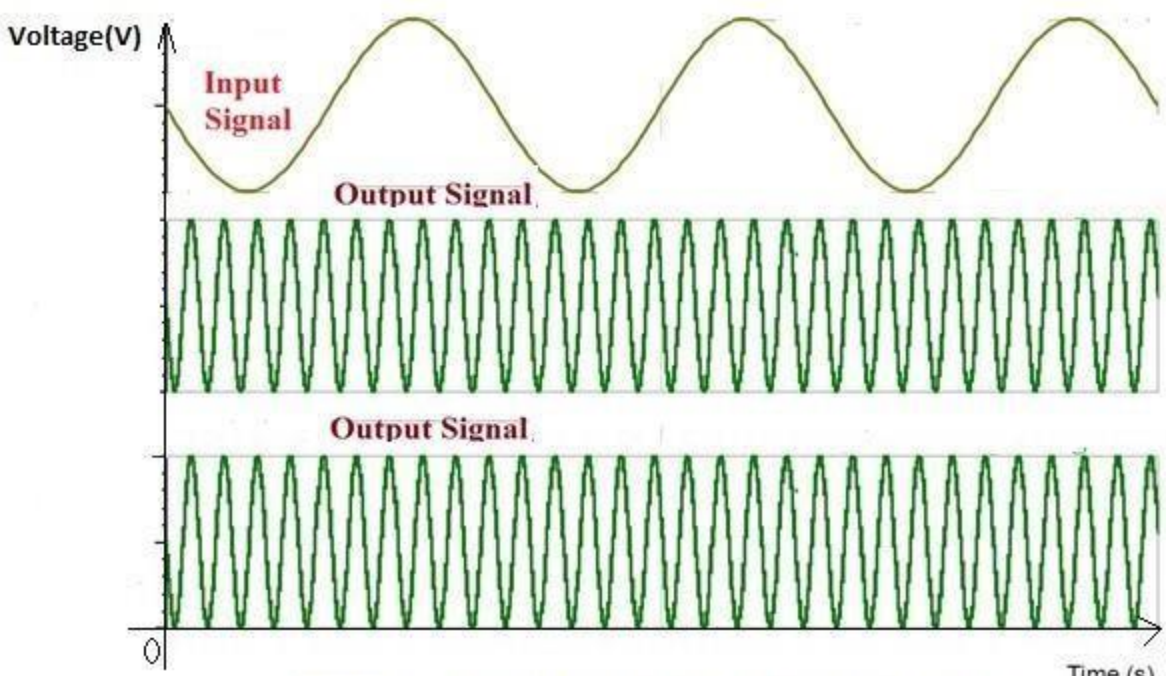


FIG: ADDER CIRCUIT FOR INPUT & OUTPUT WAVE FORMS

SUBSTRACTOR:

CIRCUIT DIAGRAM:

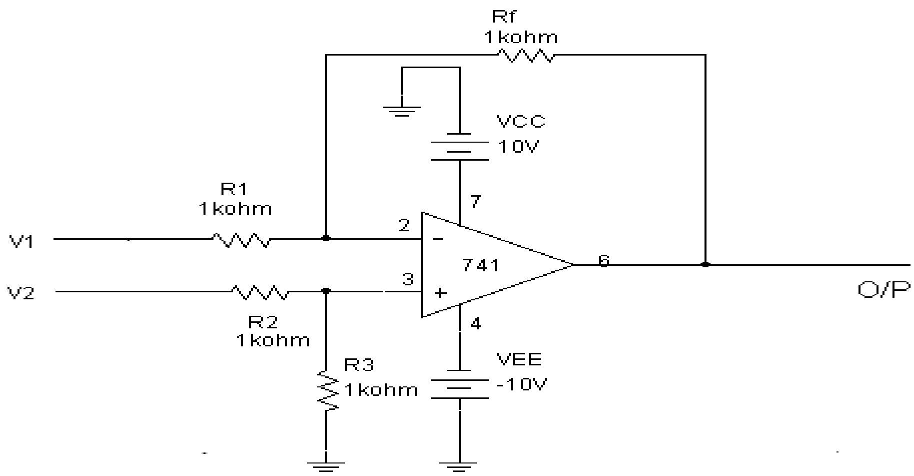


Fig: Substractor (Difference Amplifier)

THEORY:

The differential amplifier amplifies the voltage difference present on its inverting and non-inverting inputs. Thus far we have used only one of the operational amplifiers inputs to connect to the amplifier, using either the "inverting" or the "non-inverting" input terminal to amplify a single input signal with the other input being connected to ground. But as a standard operational amplifier has two inputs, inverting and no-inverting, we can also connect signals to both of these inputs at the same time producing another common type of operational amplifier circuit called a **Differential Amplifier**.

Basically, as we saw in the first tutorial about operational amplifiers, all op-amps are "Differential Amplifiers" due to their input configuration. But by connecting one voltage signal onto one input terminal and another voltage signal onto the other input terminal the resultant output voltage will be proportional to the "Difference" between the two input voltage signals of V_1 and V_2

A basic differential amplifier can be used as a subtractor. It can also be used to perform addition and subtraction with single Op-amp. From the circuit given below we will get output as Vo=(V3+V4)–(V1+V2)

PROCEDURE:

1) Connect the circuit as per given the circuit diagram.
2) The bias voltages are applied to the circuit i.e. 4th & 7th pin numbers.
3) Apply the voltages V_1 and V_2 (inverting terminal) at pin no. 2&3.
4) Observe the output d.c. voltage at pin number 6 with digital multimeter.
5) Calculate the theoretical values and compare with the practical values.

TABULAR COLUMN:

S. No.	V_2 (V)	V_1 (V)	Theoretical values(V_2-V_1)	Practical Values(V)
1	2	1	1	1.3
2	4	2	2	2.3
3	4	3	1	5.2

Design Aspects: For Substractor:

$$V_o = -R_F \frac{(V_2 - V_1)}{R_1}$$

If R_F=R_1 then V_o = V_1-V_2

Assume R_1=1kΩ

EXPECTED WAVE FORMS:

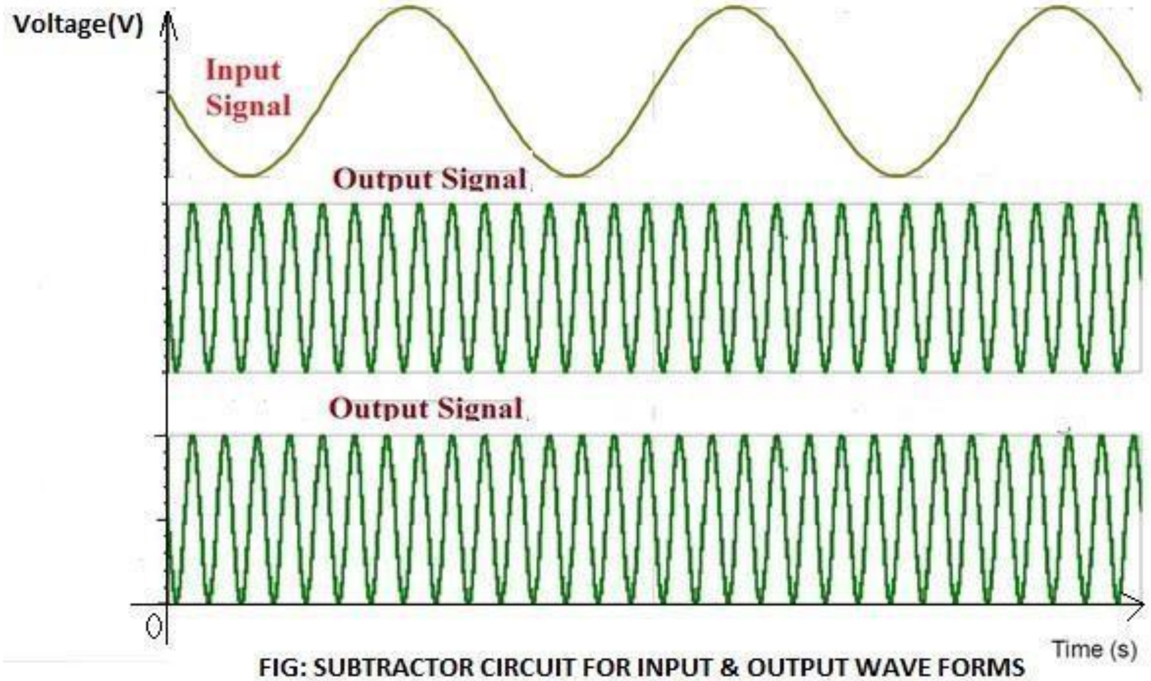


FIG: SUBTRACTOR CIRCUIT FOR INPUT & OUTPUT WAVE FORMS

Comparator circuits

AIM:

To study the following circuits, using Op-amp

APPARATUS REQUIRED:

S. No.	Name of the Apparatus	Range	Quantity
1	Function Generator	3 MHz	1
2	CRO	30 MHz	1
3	Dual Regulated Power Supply	0-30V	2
4	CRO probes	--------	2

COMPONENTS REQUIRED:

S. No.	Name of the Apparatus	Quantity
1	Resistor 100Ω	2
2	1n4007diodes	2
3	IC-741	1
4	Bread board	1
5	Connecting wires	As required

THEORY:

The **Op-amp comparator** compares one analogue voltage level with another analogue voltage level, or some preset reference voltage, V_{REF} and produces an output signal based on this voltage comparison. In other words, the op-amp voltage comparator compares the magnitudes of two voltage inputs and determines which is the largest of the two.

We have seen in previous tutorials that the operational amplifier can be used with negative feedback to control the magnitude of its output signal in the linear region performing a variety of different functions. We have also seen that the standard operational amplifier is characterized by its open-loop gain A_O and that its output voltage is given by the expression: $V_{OUT} = A_O(V+ – V-)$ where V+ and V- correspond to the voltages at the non-inverting and the inverting terminals respectively.

Voltage comparators on the other hand, either use positive feedback or no feedback at all (open-loop mode) to switch its output between two saturated states, because in the open-loop mode the amplifiers voltage gain is basically equal to A_{VO}. Then due to this high open loop gain, the output from the comparator swings either fully to its positive supply rail, +Vcc or fully to its negative supply rail, -Vcc on the application of varying input signal which passes some preset threshold value.

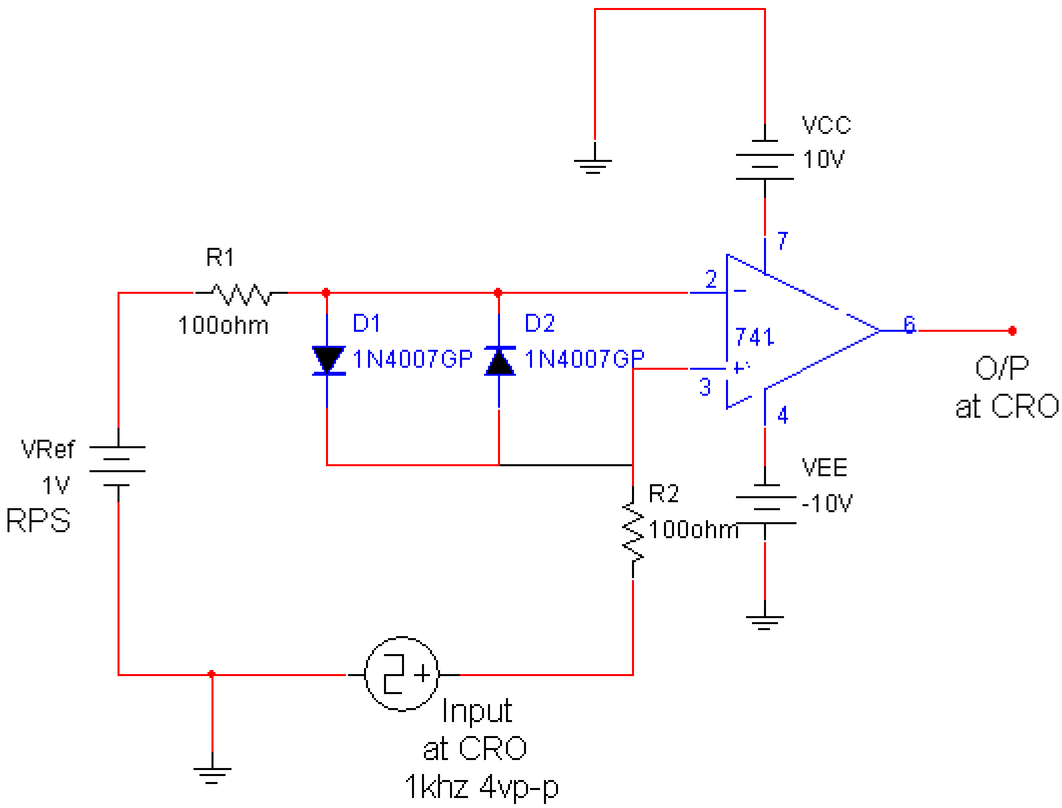
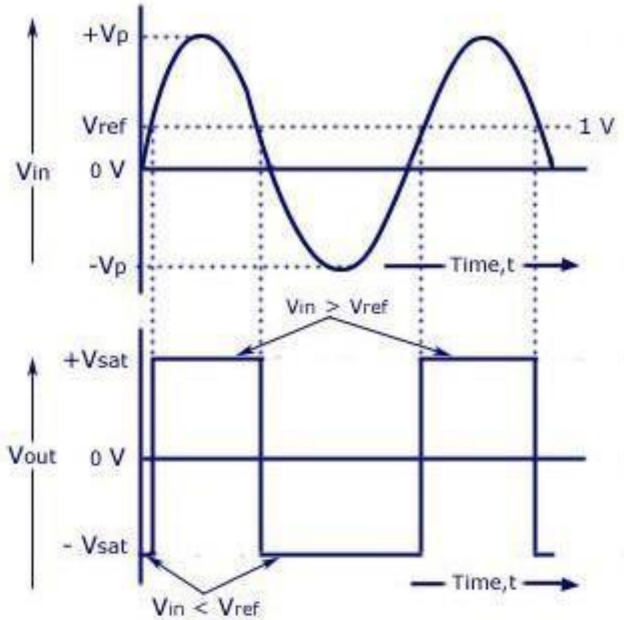


Fig: Inverting Comparator using I.C.741

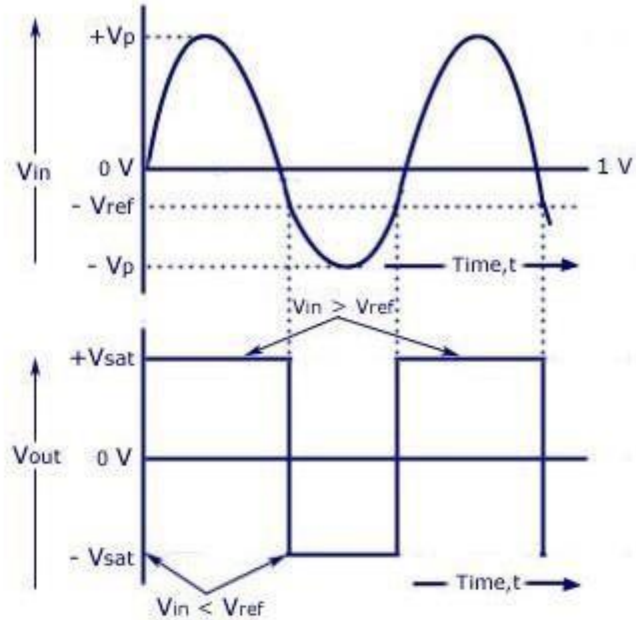
PROCEDURE:

1) Connect the circuit as per given the circuit diagram.
2) The bias voltages are applied to the both .4th & 7th pin numbers.
3) Apply a sine frequency of $4V_{P-P}$ and 1khz frequency to the Non-inverting terminal at the pin no.2.
4) Apply both channels channel 1 must be in the input and channel 2 must be in the output.
5) Apply V_{Ref} of 1V to the Inverting input terminal at pin no.3.
6) Apply V_{Ref} at different levels above and below zero axis and
7) Observe and draw the output wave forms at pin no.6.

EXPECTED WAVE FORMS:



Input and Output Waveforms
For Positive Vref



Input and Output Waveforms
For Negative Vref

TABULAR COLUMN:

S. No.	Voltage input	Vref	Observed square wave amplitude
1			
2			
3			
4			

RESULT:

OP AMP Applications – Adder, Subtractor, Comparators circuits designed and output wave forms studied.

PRECAUTIONS:

1. Precautions should be taken to insure that the power supply to the operational amplifier never becomes reversed in polarity.
2. The input voltage at the positive supply pin must be greater than the input voltage atthe negative supply pin.
3. Make null adjustment before applying the input signal.
4. Maintain proper Vcc levels.

VIVA QUESTIONS:

1. What is an op-amp?
   An operational amplifier (op-amp) is an integrated circuit (IC) that amplifies the difference in voltage between two inputs. It is so named because it can be configured to perform arithmetic operations

2. Adder is used in?
   An op-amp based adder produces an output equal to the sum of the input voltages applied at its inverting terminal. It is also called as a summing amplifier, since the output is an amplified one. In the above circuit, the non-inverting input terminal of the op-amp is connected to ground

3. What is called a Subtractor or differential amplifier?
   A differential amplifier (also known as a difference amplifier or op-amp subtractor) is a type of electronic amplifier that amplifies the difference between two input voltages but suppresses any voltage common to the two inputs

4. What is the purpose of a comparator in op amps?
   The Op-amp comparator compares one analogue voltage level with another analogue voltage level, or some preset reference voltage, V_{REF} and produces an output signal based on this voltage comparison

Experiment No: 2 **Date:**

Integrator and Differentiator Circuits using IC 741.

AIM:

To design and simulate a Integrator circuit and observe input with different output waveforms.

APPARATUS REQUIRED:

S. No.	Name of the Apparatus	Range	Quantity
1	Function Generator	3 MHz	1
2	CRO	30 MHz	1
3	Dual Regulated Power Supply	0-30V	1
4	CRO probes	--------	2

COMPONENTS REQUIRED:

S. No.	Name of the Apparatus	Quantity
1	Resistor1.369k	1
2	Capacitor1000nF(0.001uF)	1
3	IC-741	1
4	Bread board	1
5	Connecting wires	As required

SPECIFICATIONS TAKEN:

Integrator circuit design has been implemented on the virtual breadboard using following specifications:

- Power Supply: +10v and -10v
- Function generator: Selected wave with following specifications:
  Frequency:1khz
  Amplitude:2V
  Duty cycle = 50%
- Capacitor C: 1000nF
- Resistor R_1: 1.369K

THEORY:

The circuit in fig 1 is an integrator, which is also a low-pass filter with a time constant=R_1C. When a voltage, V_{in} is firstly applied to the input of an integrating amplifier, the uncharged capacitor C has very little resistance and acts a bit like a short circuit (voltage follower circuit) giving an overall gain of less than 1, thus resulting in zero output. As the feedback capacitor C begins to charge up, its reactance X_c decreases and the ratio of Z_f/R_1 increases producing an output voltage that continues to increase until the capacitor is fully charged. At this point the ratio of feedback capacitor to input resistor (Z_f/R_1) is infinite resulting in infinite gain and the output of the amplifier goes into saturation. (Saturation is when the output voltage of the amplifier swings heavily to one voltage supply rail or the other with no control in between). The circuit design generate triangular wave providing square wave as input to the integrator. Hence, the integrator circuit generates integral output with respect to the input waveform.

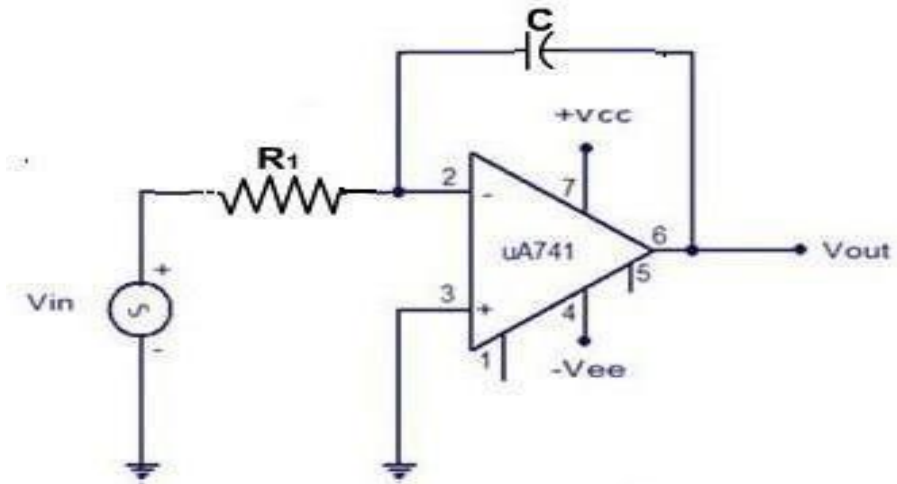


Fig: Integrator circuit

PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. Give the input signal as specified.
3. Switch on the power supply.
4. Note down the outputs from the CRO
5. Draw the necessary waveforms on the graph sheet.

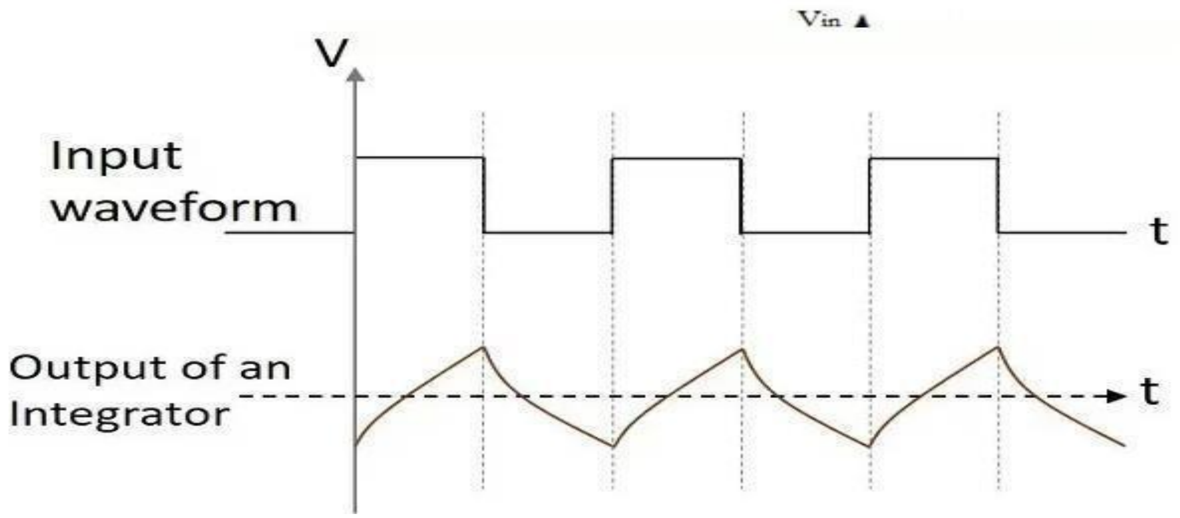
OBSERVATIONS:

1. Observe the output waveform from CRO. A square wave will generate a triangular wave and sine wave will generate a cosine wave.
2. Measure the frequency and the voltage of the output waveform in the CRO.
3. Calculate

$$V_o = -\frac{1}{R_1 C}\int V_{in}\, dt$$

4. Compare the calculated output voltage with the experimentally observed voltage from the output waveform.
5. Observe outputs of the integrator circuit using different input waveforms.

EXPECTED WAVE FORMS:



LAB OBSERVATIONS TAKEN:

For example, a case has been taken and the required parameters values is being noted down below:

1. Input Voltage: 2.09V
2. Frequency: 50Hz
3. Output Voltage: 4.31V
4. Phase Difference: -92

CALCULATIONS:

If input V_{in} = 2.09 sin (2*50*t)
Output of the integrator will be equal to

$$V_o = -\frac{1}{R_1 C}\int V_{in\,dt}$$

Thus,

$$V_o = -\frac{1}{1.369\times 10^{3}\times 10^{-6}}\int 2.09\sin(100\pi t)\,dt$$

$$V_o = -\frac{2.09}{1.369\times 10^{-3}\times 100\pi}[-\cos(100\pi t)]$$

$$V_o = 4.72\cos(100\pi t)$$

OBSERVATIONS:

S.No	Input Waveform	Time period	Amplitude	Output waveform	Amplitude	Time period
1	Square wave					
2	Saw tooth wave					

AIM:

To design and simulate a Differentiator circuit and observe input with different output waveforms.

APPARATUS REQUIRED:

S. No.	Name of the Apparatus	Range	Quantity
1	Function Generator	3 MHz	1
2	CRO	30 MHz	1
3	Dual Regulated Power Supply	0-30V	1
4	CRO probes	--------	2

COMPONENTS REQUIRED:

S. No.	Name of theApparatus	Quantity
1	Resistor10.38k	1
2	Capacitor(1000nF)0.001µf	1
3	IC-741	1
4	Bread board	1
5	Connecting wires	As required

LAB SPECIFICATIONS TAKEN:

Integrator circuit design has been implemented on the virtual breadboard using following specifications:

- Power Supply: +10v and -10v
- Function generator: Selected wave with following specifications:
  Frequency = 45Hz, 50Hz, 55Hz, 60Hz, 100Hz.
  Amplitude: 2V
  Duty cycle = 50%
- Capacitor C: 1000nF
- Resistor R_1: 10.38K

THEORY:

The basic Differentiator Amplifier circuit is the exact opposite to that of the Integrator operational amplifier circuit that we saw in the previous experiment. Here, the position of the capacitor and resistor have been reversed and now the Capacitor, C is connected to the input terminal of the inverting amplifier while the Resistor, R_1 forms the negative feedback element across the operational amplifier. This circuit performs the mathematical operation of Differentiation that is it produces a voltage output which is proportional to the input voltage's rate-of-change and the current flowing through the capacitor. Or in other words the output voltage is a scaled version of the derivative of the input voltage. The capacitor blocks any DC content only allowing AC type signals to pass through and whose frequency is dependent on the rate of change of the input signal. At low frequencies the reactance of the capacitor is "High" resulting in a low gain (R_1/X_c) and low output voltage from the op-amp.

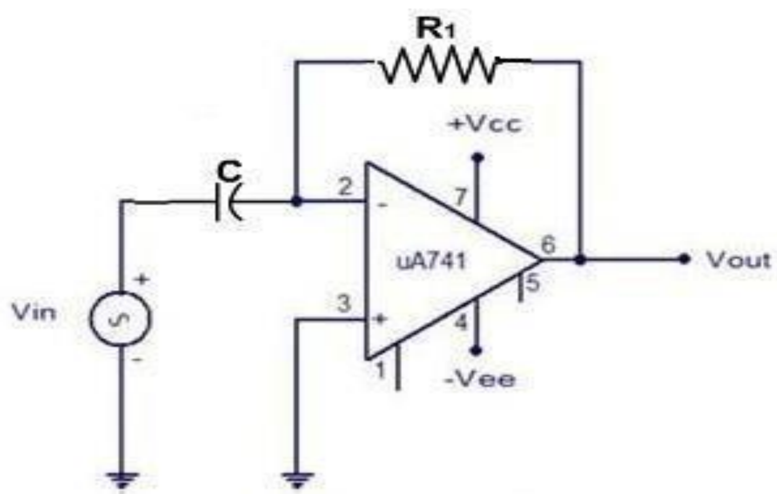


Fig: Differentiator circuit

PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. Give the input signal as specified.
3. Switch on the power supply.
4. Note down the outputs from the CRO
5. Draw the necessary waveforms on the graph sheet.

OBSERVATIONS:

1. Observe the output waveform from CRO.
2. Measure the frequency and the voltage of the output waveform in the CRO.
3. Check

$$V0 = -R_1C\frac{dV_{in}}{dt}$$

4. Frequency of the output waveform will remain same and the output voltage can be calculated using above equation and compared with the observed value.

5. Observe outputs of the differentiator circuit using different input waveforms.

EXPECTED WAVE FORMS:

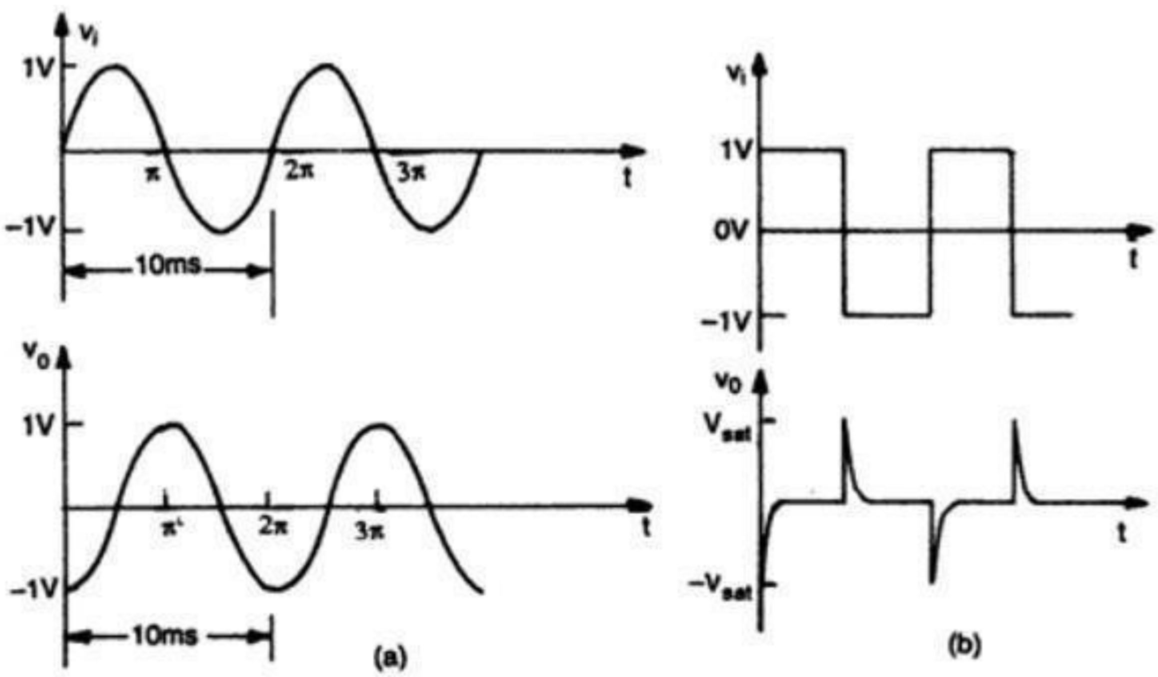


Fig. (a) Sine-wave input and cosine output (b) Square wave input and spike output

Fig: Output wave forms for Differentiator

LAB OBSERVATIONS OBTAINED:

For example, a case has been taken and the required parameters values is being noted down below:

1. Input Voltage: 3.13V
2. Frequency: 45Hz
3. Output Voltage: 4.31VV
4. Phase Difference: 97

TABULAR FORM:

S.No	Input Waveform	Time period	Amplitude	Output waveform	Amplitude	Time period
1	Sine wave					
2	Cosine wave					

CALCULATIONS:

If input V_{in} = 3.13 sin (2*45*t)
Output of the integrator will be equal to

$$V0=-R_1C\frac{dV_{in}}{dt}$$

$$V0=-10.38x10^3x10^{-6}\frac{d(3.13\sin(90\pi t))}{dt}$$

V0=8.93 cos (90ϖt)

-

RESULT:

Integrator and Differentiator circuits designed and output waveforms have been studied.

PRECAUTIONS:

1. Precautions should be taken to insure that the power supply to the operational amplifier never becomes reversed in polarity.
2. The input voltage at the positive supply pin must be greater than the input voltage at the negativesupply pin.

VIVA QUESTIONS &ANSWERS:

1. What factor makes differentiator?

The value of internal resistor and capacitor and feedback resistor and capacitor of the differentiator values should be selected such that f_ab c to make the circuit more stable.

2. Why capacitor is used in differentiator?

The input signal to the differentiator is applied to the capacitor. The capacitor blocks any DC content so there is no current flow to the amplifier summing point, X resulting in zero output voltage.

3. What is differentiator circuit?

The differentiator circuit outputs the derivative of the input signal over a frequency range based on the circuit time constant and the bandwidth of the amplifier. The input signal is applied to the inverting input so the output is inverted relative to the polarity of the input signal.

4. Applications of differentiator and integrator?

The differentiator circuit outputs the derivative of the input signal over a frequency range based on the circuit time constant and the bandwidth of the amplifier. The input signal is applied to the inverting input so the output is inverted relative to the polarity of the input signal

Experiment No: 3 **Date:**

Active Filter Applications – LPF, HPF (first order)

AIM:

1) To design low pass and high pass filter of first order.
2) To study the frequency response of first order low pass and high pass filters using IC-741.

APPARATUS REQUIRED:

S. No.	Name of the Apparatus	Range	Quantity
1	Function Generator	3 MHz	1
2	CRO	30 MHz	1
3	Dual Regulated Power Supply	0-30V	1
4	CRO probes	--------	2

COMPONENTS REQUIRED:

S. No.	Name of the Apparatus	Quantity
1	Resistors 10 kΩ	2
2	Potentiometer (pot) 10 kΩ	1
3	Capacitor 0.01μf	1
4	I.C. 741	1
5	Bread board	1
6	Connecting wires	As required

THEORY:

By combining a basic RC Low Pass Filter circuit with an operational amplifier we can create an Active Low PassFilter circuit complete with amplification

In the RC Passive Filter tutorials, we saw how a basic first-order filter circuits, such as the low pass and the high pass filters can be made using just a single resistor in series with a non-polarized capacitor connected across a sinusoidal input signal.

We also noticed that the main disadvantage of passive filters is that the amplitude of the output signal is less thanthat of the input signal, ie, the gain is never greater than unity and that the load impedance affects the filters characteristics.

With passive filter circuits containing multiple stages, this loss in signal amplitude called "Attenuation" can become quiet severe. One way of restoring or controlling this loss of signal is by using amplification through the use of **Active Filters**.

An Active High Pass Filter can be created by combining a passive RC filter network with an operational amplifier toproduce a high pass filter with amplification

Technically, there is no such thing as an **active high pass filter**. Unlike Passive High Pass Filters which have an "infinite" frequency response, the maximum pass band frequency response of an active high pass filter is limited by the open-loop characteristics or bandwidth of the operational amplifier being used, making them appear as if they are band pass filters with a high frequency cut-off determined by the selection of op-amp and gain.

In the Operational Amplifier tutorial we saw that the maximum frequency response of an op-amp is limited to theGain/Bandwidth product or open loop voltage gain (A_V) of the operational amplifier being used giving it a bandwidth limitation, where the closed loop response of the op amp intersects the open loop response

CIRCUIT DIAGRAM:

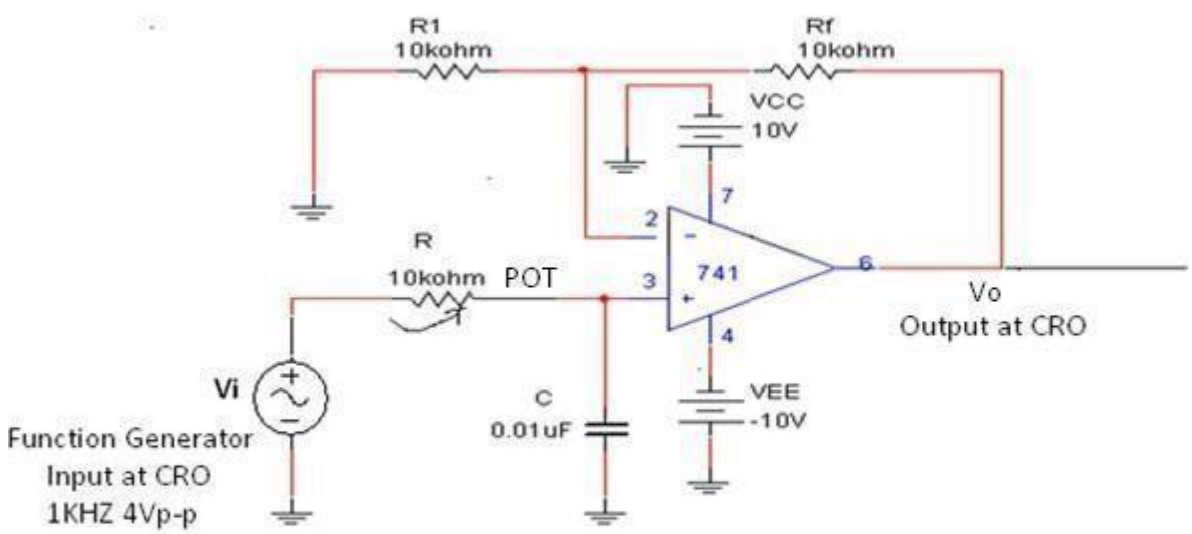


FIG: LOW PASS FILTER USING 741 I.C.

PROCEDURE:

For low pass filter

1) Connect the circuit as per the circuit diagram.
2) The bias voltages are applied to the circuit i.e. 4^{th} and 7^{th} pin numbers.
3) Using function generator, adjust the amplifier of input sinusoidal voltage to $4V_{P-P.}$
4) Vary the frequency from 30 HZ to 30 KHZ note down output voltage by observing wave forms on C.R.O.
5) Calculate gain i.e., $20\log(\frac{V_o}{V_{in}})$
6) Plot the graph between frequency and voltage gain.

7) Compare theoretical and practical cut-off frequencies.

DESIGN:

1) Low pass filter: F_H= higher cut-off frequency = $\frac{1}{2\Pi RC}$

Let F_H= 1 KHZ

Pass band A_F = 2

Select C = 0.01µf

$R = \frac{1}{2\Pi RC} = 15.9k\Omega$

$A_F = 1 + \frac{R_F}{R_1} = 2$

$R_F = 1R_1$

Choose 10KΩ

=10KΩX1

R_F =10kΩ

2) High pass filter: F_L = lower cut-off frequency = $\frac{1}{2\Pi RC}$

$A_F = 1 + \frac{R_F}{R_1}$

F_L= 1 KHZ

C = 0.01µf A_F=2

R = 15.9kΩ

TABULAR COLUMN: 1) For Low Pass Filter

Let $V_{IN} = 2\ V_{P-P}$

Sl.No	Input frequency	Output voltage	Gain	20 log Vo/Vi
1.				
2				
3				
4.				
5.				
6.				
7.				
8.				
9.				
10.				
11.				

CIRCUIT DIAGRAM:

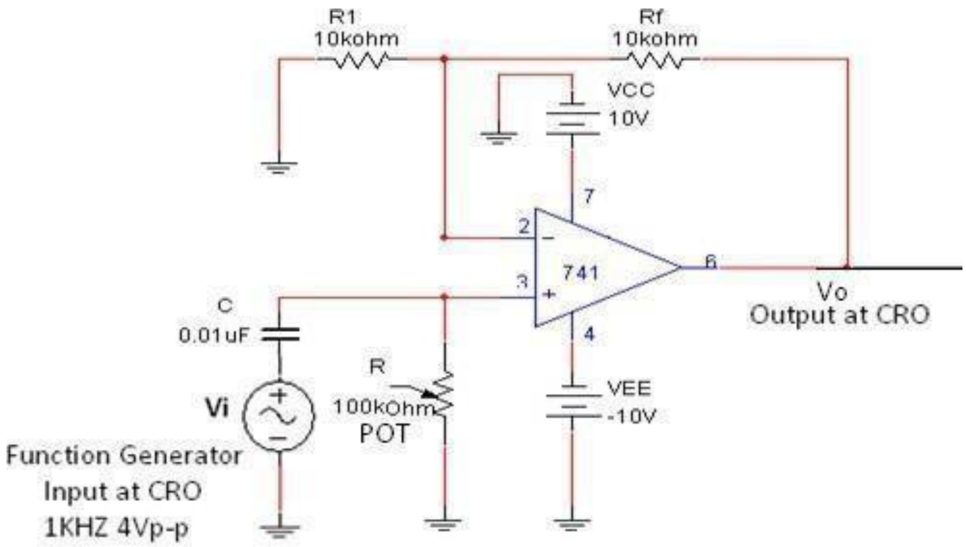


FIG: HIGH PASS FILTER USING 741 I.C.

PROCEDURE:

For high pass filter

1) Connect the circuit as per given the circuit diagram.
2) The bias voltages are applied to the circuit i.e. 4th and 7th pin numbers.
3) Using function generator, adjust the amplifier of input sinusoidal voltage to 4 $V_{P-P.}$
4) Vary the frequency from 30 HZ to 30 KHZ and note down output voltage by observing wave forms on C.R.O.
5) Calculate gain i.e., $20\log(\frac{V_o}{V_{in}})$.
6) Plot the graph between frequency verses voltage gain.
7) Compare theoretical and practical cut-off frequencies

TABULAR COLUMN:

Let $V_{IN} = 2V_{P-P}$

Sl.No	Input frequency	Output voltage	Gain	20 log Vo/Vi
1.				
2				—
3				
4.				
5.				
6.				
7.				
8.				
9.				
10.				
11.				

EXPECTED WAVE FORMS:

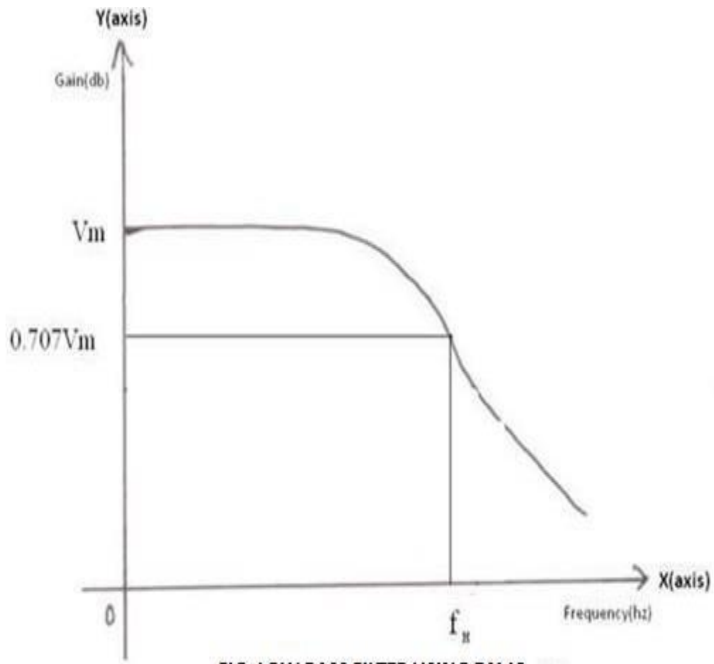


FIG: LOW PASS FILTER USING 741 IC

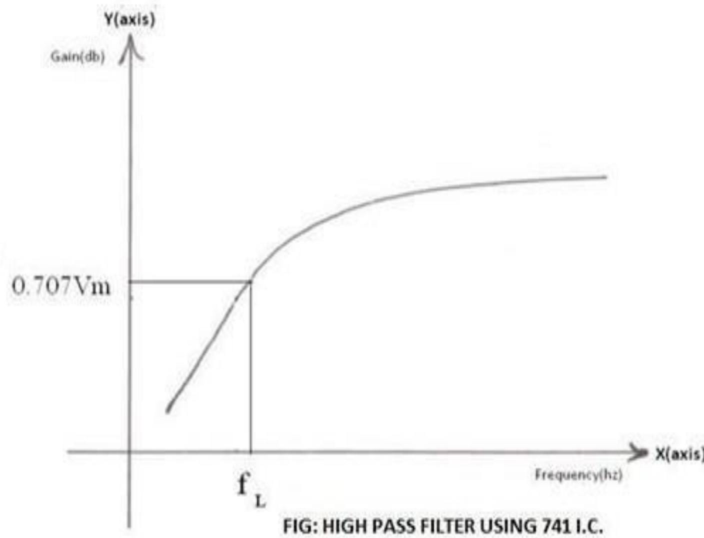


FIG: HIGH PASS FILTER USING 741 I.C.

RESULT:

We studied and designed the low pass and high pass filter of first order using IC-741 and graph is drawnand output voltages is observed.

PRECAUTIONS:

1. Make null adjustment before applying the input signal.
2. Maintain proper Vcclevels.

VIVA QUESTIONS:

1. What is a low-pass filter?

   A low-pass filter (LPF) is a circuit that only passes signals below its cutoff frequency while attenuating all signals above it. It is the complement of a high-pass filter, which only passes signals above its cutoff frequency and attenuates all signals below it

2. What is the difference between LPF and HPF?

A low-pass filter (LPF) is a circuit that only passes signals below its cutoff frequency while attenuating all signals above it. It is the complement of a high-pass filter, which only passes signals above its cutoff frequency and attenuates all signals below it

3. What is the purpose of a high pass filter?
   High pass filter is used to remove unwanted sounds near to the lower end of the audible range. To prevent the amplification of DC current that could harm the amplifier, high pass filters are used for AC-coupling.

4. What are the applications of LPF&HPF?
   Applications of Active Low Pass Filters are in audio amplifiers, equalizers or speaker systems to direct the lower frequency bass signals to the larger bass speakers or to reduce any high frequency noise or “hiss” type distortion

Experiment No: 4 **Date:**

IC 741 Waveform Generators – Sine, Square wave and Triangular waves.

AIM:

To generate sine, triangular and square waveforms and to determine the Frequency of oscillations.

APPARATUS REQUIRED:

S. No.	Name of the Apparatus	Range	Quantity
1	Function Generator	3 MHz	1
2	CRO	30 MHz	1
3	Dual Regulated Power Supply	0-30V	1
4	CRO probes	--------	2

COMPONENTS REQUIRED: For sine & square wave

S. No.	Name of the Apparatus	Quantity
1	Resistor 470kΩ	1
2	Resistors 10 kΩ	2
3	Potentiometer 1 kΩ	3
4	Capacitor 0.1µf	3
5	I.C. 741	1
6	Bread board	1
6	Connecting wires	As required

For Triangular wave:

S. No.	Name of the Apparatus	Quantity
1	Resistor 1kΩ	1
2	Resistor 1MΩ	1
3	Resistors 10 kΩ	2
4	Capacitor 0.01µf	2
5	I.C. 741	2
6	Bread board	1
6	Connecting wires	As required

CIRCUIT DIAGRAMS:

SINE WAVE GENERATOR: (RC PHASE SHIFT OSCILLATOR)

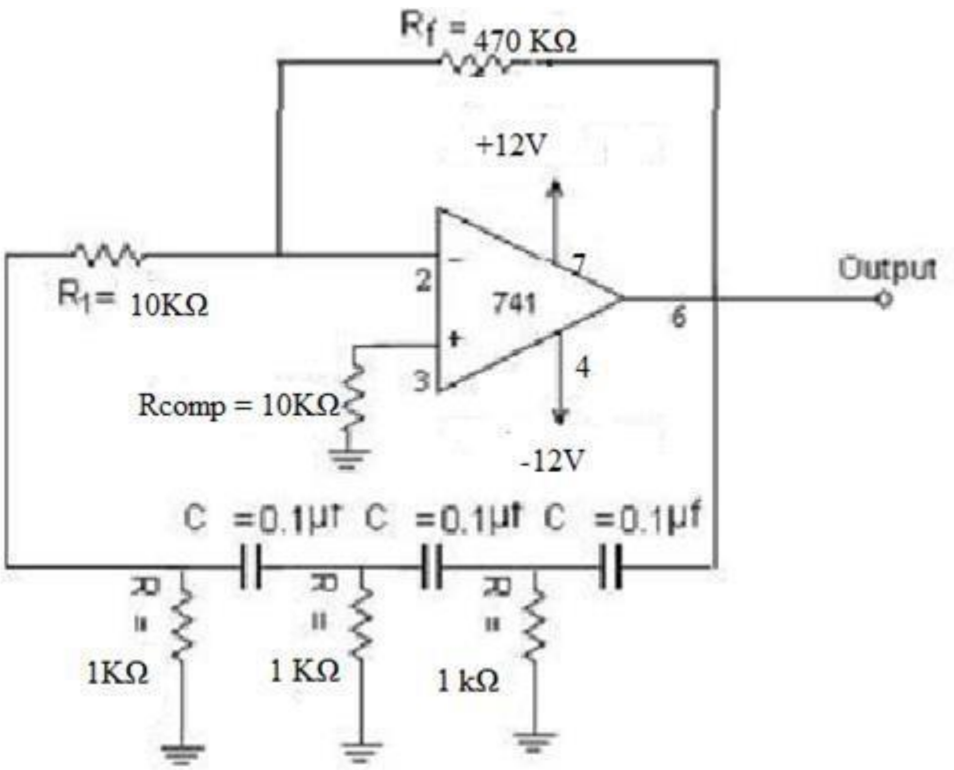


Fig - 1

SQUARE AND TRIANGULAR WAVE GENERATOR:

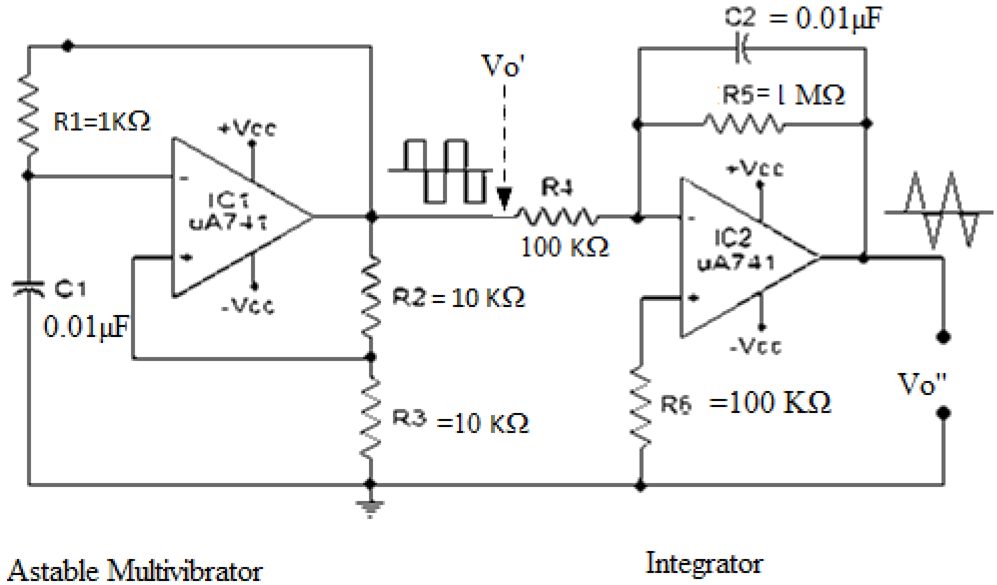


Fig - 2

THEORY:

RC oscillator is build using an amplifier and a RC network in feedback. For any oscillator the two prime requirements to generate sustained and constant oscillations are

1. The total phase shift around loop must be 0^0 or 360^0 degrees.
2. The loop gain should be equal to unity.

This is known as "*Barkhausen Criterion*"

In RC phase shift oscillator op-amp is used as an amplifier in inverting configuration. It gives 180^o phase shift in its output. So the RC feedback network following the amplifier has to produce additional 180^o phase shift to make total phase shift $360^o / 0^o$.

The circuit oscillates at a frequency $F = 1 / 2\pi RC\sqrt{6}$

The time period of the output of the uA741 square wave generator can be expressed using the following equation:

$$T = 2 \times 2.303\, R_1C_1 \log_{10} \left(\frac{2R_3 + R_2}{R_2}\right) \text{ Second}$$

The common practice is to make the R_3 equal to R_2. Then the equation for the time period can be simplified as: $T = 2.1976R_1C_1$

The frequency can be determined by the equation: F = 1/T

PROCEDURE:

For Sine Wave Generation:

1. Connect the circuit as per the circuit diagram shown in Fig 1.
2. Give +12V, -12V and ground to circuit from power supply
3. Observe the output on the CRO.
4. Calculate theoretical and practical output signal frequency and compare them.

For Square and Triangular Wave Generation:

1. Connect the circuit as per the circuit diagram shown in Fig 2.
2. Observe square wave at Vo' and Triangular wave at Vo" as shown in figure 3.
3. Plot the waveforms on the graph sheet.
4. Calculate the frequency theoretically and compare them with the practical one.

EXPECTED WAVEFORMS:

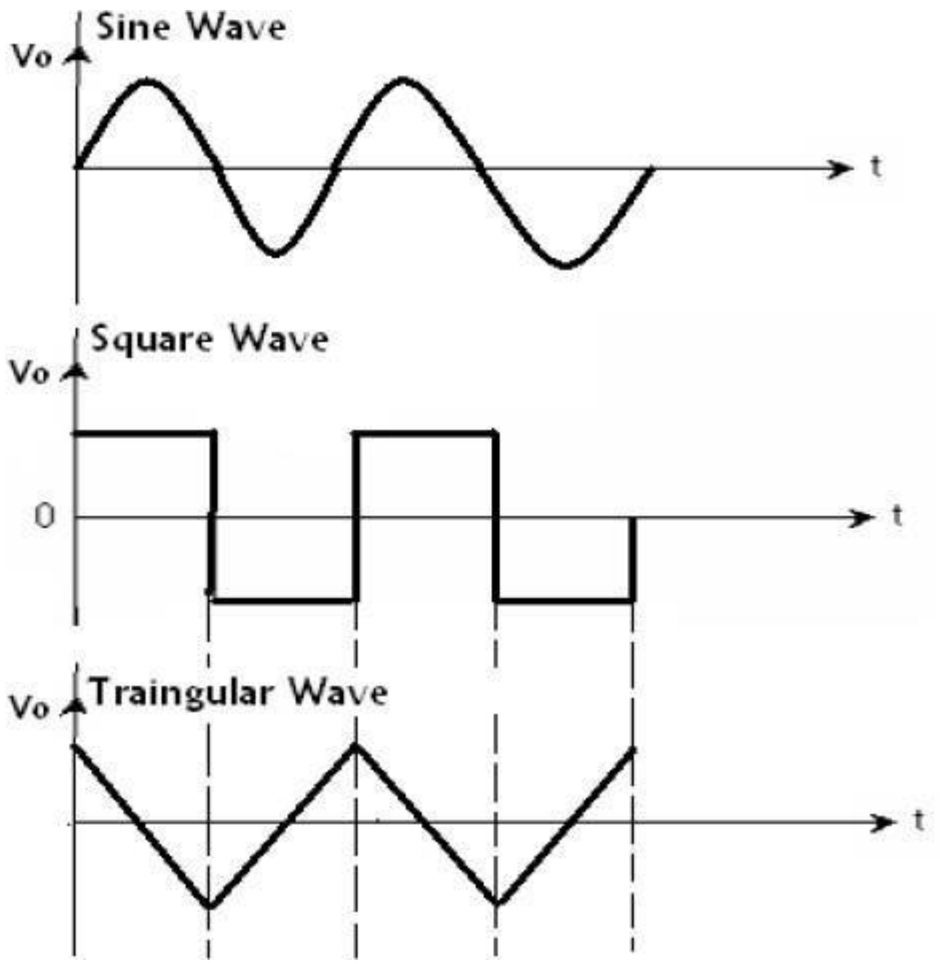


Fig - 3.

RESULT:

Designed and studied the sine, triangular and square waveforms and observed the Frequency of oscillations, output wave forms drawn.

PRECAUTIONS:

1. Check the circuit connections before switching on the power supply.
2. Pin No.1 and Pin No.8 should be left free.
3. Check the continuity of the connecting wires.

VIVA QUESTIONS:

1. What are the different ways of generating Sinusoidal waves?
   High pass filter is used to remove unwanted sounds near to the lower end of the audible range. To prevent the amplification of DC current that could harm the amplifier, high pass filters are used for AC-coupling.

2. What are different ways of generating square wave voltage waveforms?
   High pass filter is used to remove unwanted sounds near to the lower end of the audible range. To prevent the amplification of DC current that could harm the amplifier, high pass filters are used for AC-coupling

3. How a triangular wave can be generated?
   High pass filter is used to remove unwanted sounds near to the lower end of the audible range. To prevent the amplification of DC current that could harm the amplifier, high pass filters are used for AC-coupling

Experiment No: 5 **Date:**

IC 555 Timer – Monostable and Astable Multivibrator Circuits.

AIM: To design the monostable multivibrator circuit and using Op-Amp and IC 555.

APPARATUS REQUIRED:

S. No.	Name of the Apparatus	Range	Quantity
1	Function Generator	3 MHz	1
2	CRO	30 MHz	1
3	Regulated DC power supply	0-30V	1
4	CRO probes	--------	2

COMPONTNTS REQUIRED:

S. No.	Name of the Apparatus	Quantity
1	(R1pot.)100kΩ	1
2	Capacitor 0.1µf	1
3	Capacitor 0.01µf	1
4	Connecting wires	As required

THEORY:

We have seen that Multivibrators and CMOS Oscillators can be easily constructed from discrete components to produce relaxation oscillators for generating basic square wave output waveforms. But there are also dedicated IC's especially designed to accurately produce the required output waveform with the addition of just a few extra timing components.

One such device that has been around since the early days of IC's and has itself become something of an industry "standard" is the **555 Timer Oscillator** which is more commonly called the **"555 Timer"**.

The basic **555 timer** gets its name from the fact that there are three internally connected 5kΩ resistors which it uses to generate the two comparators reference voltages. The 555 timer IC is a very cheap, popular and useful precision timing device which can act as either a simple timer to generate single pulses or long time delays, or as a relaxation oscillator producing a string of stabilized waveforms of varying duty cycles from 50 to 100%.

CIRCUIT DIAGRAM:

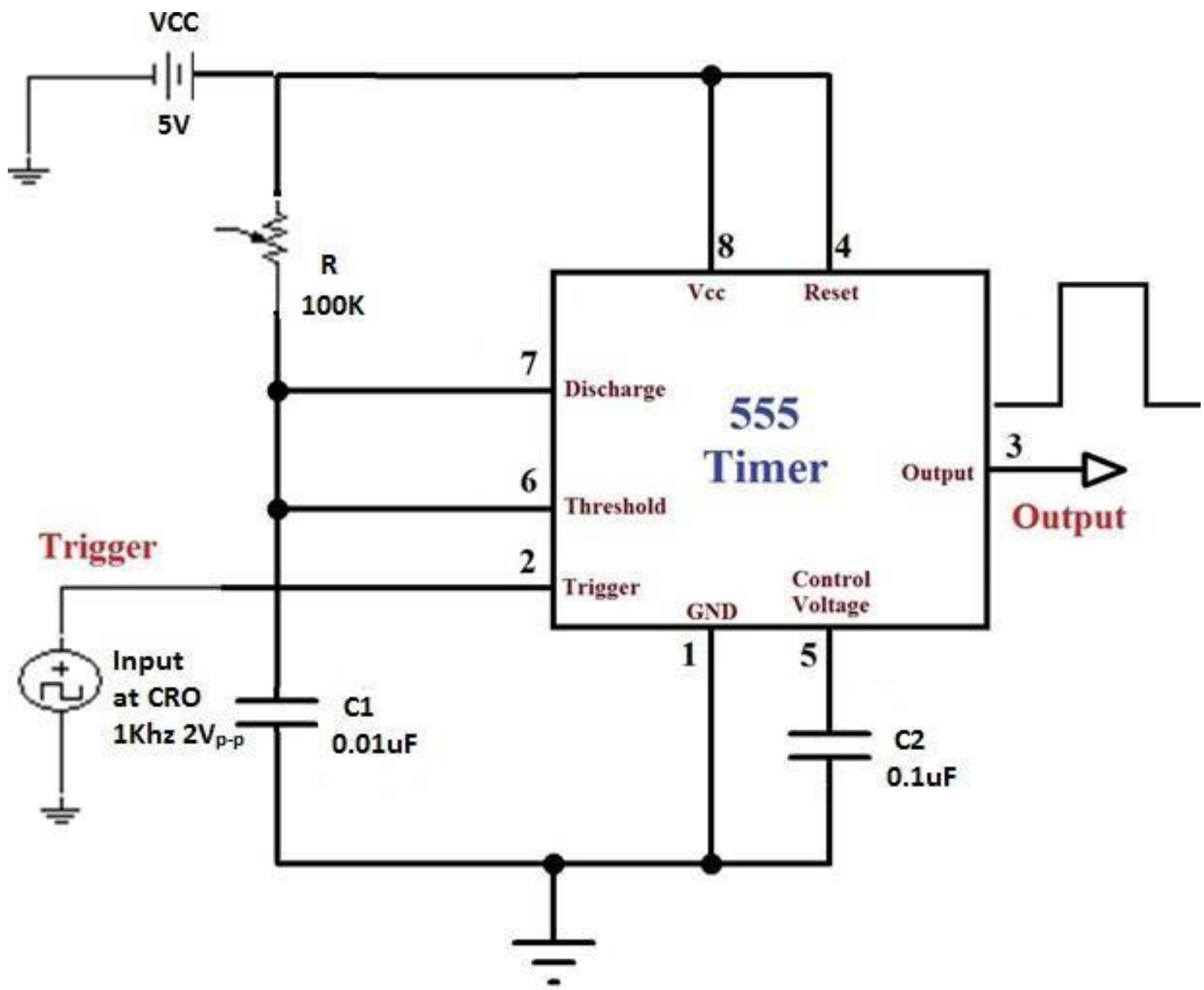


FIG: MONOTABLE MULTIVIBRATOR USING 555 IC TIMER

DESIGN:

T_p= 1.1 RC, Given T_p = 1.1msec and choose C = 0.01µf

1.1msec = 1.1 X R X 0.01µf

$$R = \frac{1.1X10^{-3}}{1.1X\,0.01X10^{-6}} = 100k\Omega$$

PROCEDURE:

1) Connect the circuit as per given the circuit diagram.
2) Apply both channels i.e. channel 1 input and channel 2 at the output.
3) Apply a square input of 4V_{P-P} and 1khz frequency at pin no.2
4) Observe the wave form at pin no.3 is(Inverter wave form) and also voltage across capacitor at pin no.6
5) Plot the wave forms at pin no.3 and pin no.6
6) Calculate theoretical values and compare them with the practical values.

THEORITICAL VALUES:

T_P=1.1RC

1.1x100x1000x.0.1x10^{-6}

=1.1msec.

PRACTICAL VALUES:

Amplitude=

Timeperiod=

Across capacitor:

Amplitude=

Time period=

EXPECTED WAVE FORMS:

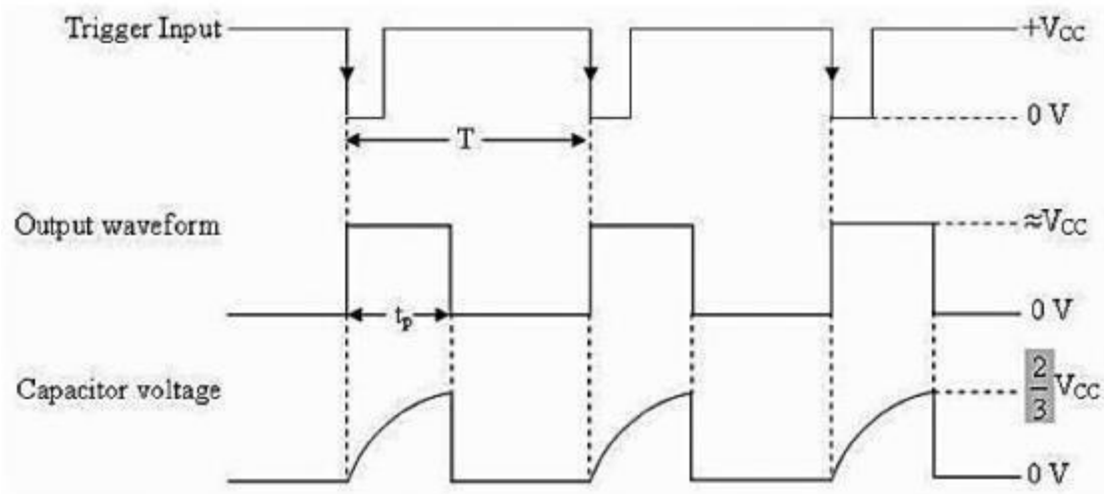


Fig: Output wave forms of Monostable 555-I.C.

PRECAUTIONS:

1. All parameters and circuit were checked firstly
2. Whole circuit was arranged tightly and carefully.
3. Calibrate the oscilloscope more accurately.
4. Supply voltage is fixed at a point and not more than 15V.
5. Readings were taken very carefully.

VIVA QUESTIONS:

1. What is a 555 IC?
   The 555 timer IC is an integrated circuit (chip) used in a variety of timer, delay, pulse generation, and oscillator applications. Derivatives provide two (556) or four (558) timing circuits in one package. The design was first marketed in 1972 by Signetics.

2. Why the Reset pin of ic 555 is normally connected to Vcc?
   The 555 timer IC is an integrated circuit (chip) used in a variety of timer, delay, pulse generation, and oscillator applications. Derivatives provide two (556) or four (558) timing circuits in one package. The design was first marketed in 1972 by Signetics.

3. Why the control voltage pin (pin 5) of 555 timers is connected to ground through a 0.01μf capacitor?
   The control pin on the 555 timers is normally connected to the ground through a capacitor (~ 0.01μF because the noise from the supply line can ride through this simple divider adding small capacitor filters out high-frequency noise that can cause the comparison point to vary slightly.

4. What is barkhausen criterion for oscillations?
   The Barkhausen criterion states that: The loop gain is equal to unity in absolute magnitude, that is, $|\beta A| = 1$ and Page 2 • The phase shift around the loop is zero or an integer multiple of 2π radian (180°) i.e. The product β A is called as the "loop gain".

AIM:

To design and study the operation of IC 555 timer as an astable multivibrator

APPARATUS REQUIRED:

S. No.	Name of the Apparatus	Range	Quantity
1	Function Generator	3 MHz	1
2	CRO	30 MHz	1
3	Regulated DC power supply	0-30V	1
4	CRO probes	--------	2

COMPONTNTS REQUIRED:

S. No.	Name of the Apparatus	Quantity
1	Resistor 2.9kΩ	1
2	Resistor 5.8kΩ	1
3	Capacitor 0.1µf	1
4	Capacitor 0.01µf	1
5	Connecting wires	Few No.
6	Bread board	1
7	555 IC	1

THEORY:

A multivibrator is a one type of electronic circuit that is used to implement a two state system like flip-flops, timers and oscillators. Multivibrators are categorized by two amplifying devices like electron tubes, transistors and other devices like capacitors and cross coupled by resistors. Multivibrators are classified into three types based on the circuit operation, namely Astable multivibrators, Bistable multivibrators and Monostable multivibrators. The astable multi vibrator is not stable and it repeatedly switches from one state to the other. In monostable multivibrator, one state is stable and remaining state is unstable. A trigger pulse is the root to the circuit to enter the unstable state. When the circuit enters into the unstable state, then it will return to the normal state after a fixed time. A bistable mutivibrator circuit is stable that can be changed from one stable to other stable by an external trigger pulse. This multi vibrator circuit is also called as flip-flop which can be used to store one bit of data.

CIRCUIT DIAGRAM:

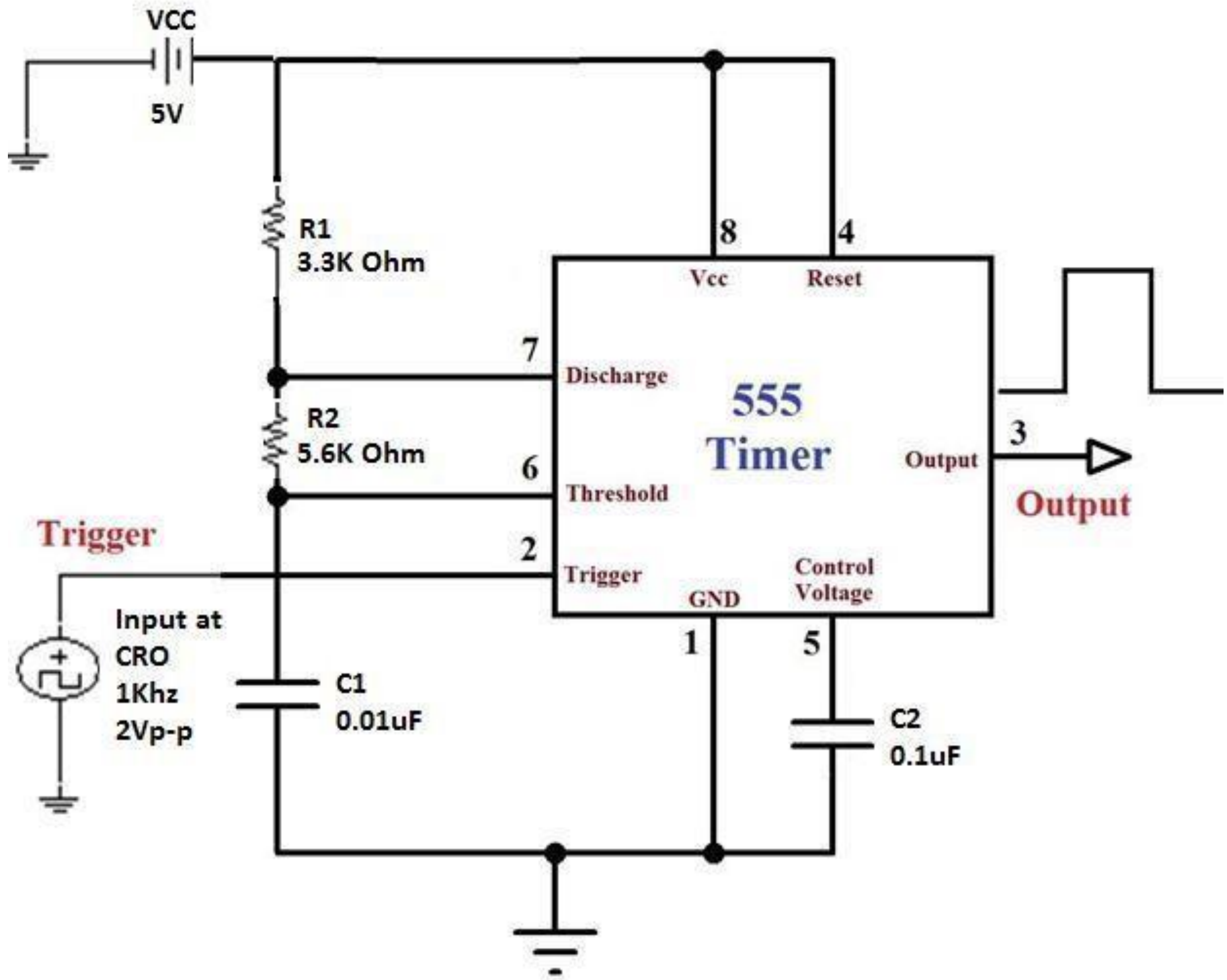


FIG: ASTABLE MULTIVIBRATOR USING 555 IC TIMER

DESIGN:

Given F = 1 KHZ assume C = 0.1µf

T_{ON} = 0.69 (R_A+R_B) CT_{OFF}=0.69R_BC

Duty Cycle= $\frac{T_{ON}}{T_{ON}+T_{OFF}}$

PROCEDURE:

1) Connect the circuit as per given the circuit diagram.
2) Observe the output wave forms at pin no.3 and pin no.6.
3) Plot the wave forms at pin no.3 and pin no.6.
4) Observe 1/3 V_{CC} and 2/3 V_{CC} and note down the peak to peak voltages

DESIGN:

Given F = 1 KHZ assume C = 0.1µf

T_{ON} = 0.69 (R_A+R_B) CT_{OFF}=0.69R_BC

Duty Cycle= $\frac{T_{ON}\, T_{ON}}{+T_{OFF}} = \frac{0.69(R_A + R_B)C}{0.69(R_A + 2R_B)C}$

$0.69\ (R_A+2R_B) = R_A+R_B$

$0.5\,R_A=0.2R_B$

$$\frac{R_A}{R_B} = \frac{1}{2}$$

Then $2R_A = R_B$

$$1\ KHZ = \frac{1.45}{(R_A + 2R_B)C}$$

$$R_A = \frac{1.45}{(R_A + 4R_A)C}$$

$$R_B = \frac{1.45}{5R_AC}$$

$=2.9\ k\Omega$

$2R_A=2X2.9=5.8\ k\Omega$

$$\%\ \text{of Duty Cycle} = \frac{R_A + R_B}{R_A + 2R_B} X100$$

EXPECTED WAVE FORMS:

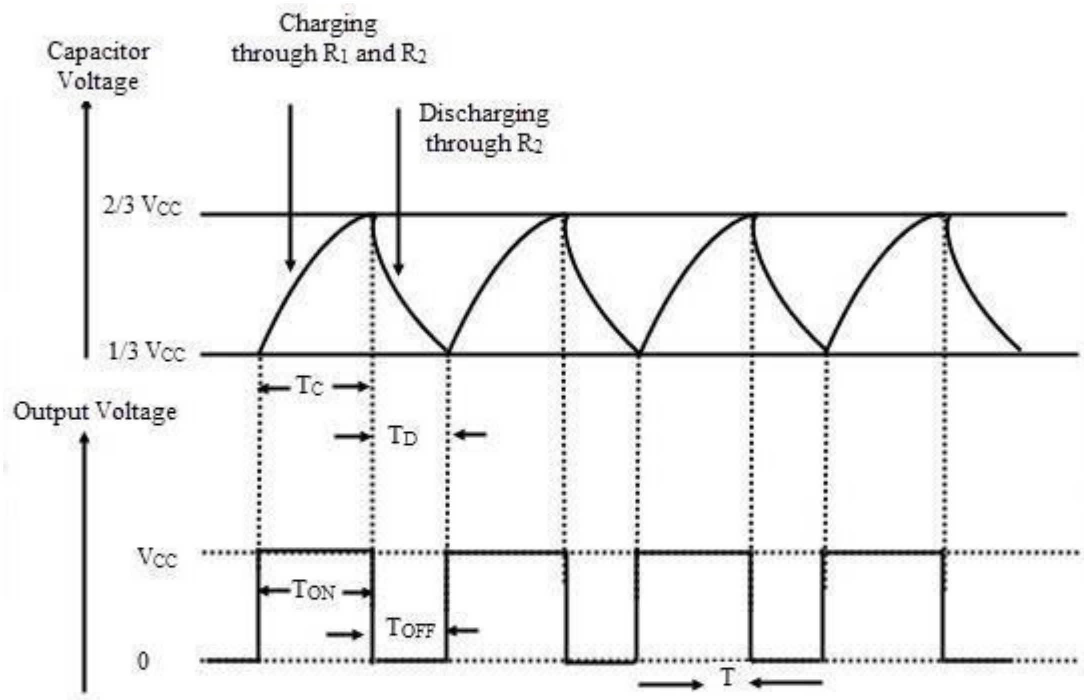


Fig: Output wave forms of Astable multivibrator using 555-I.C.

PRACTICAL VALUES:

Amplitude=

Time period=

Across capacitor:

Amplitude=

Time period=

RESULT:

Monostable & Astable multivibrator circuits designed and studied the performance practically by using 555 timer

PRECAUTIONS:

1. All parameters and circuit were checked firstly
2. Whole circuit was arranged tightly and carefully.
3. Calibrate the oscilloscope more accurately.
4. Supply voltage is fixed at a point and not more than 15V.
5. Readings were taken very carefully.

VIVA QUESTIONS:

1. Write the formula to calculate the time period of the astable?

   Then taking one side of the astable multivibrator, the length of time that transistor TR_2 is "OFF" will be equal to 0.69T or 0.69 times the time constant of C1 x R3. Likewise, the length of time that transistor TR_1 is "OFF" will be equal to 0.69T or 0.69 times the time constant of C2 x R2 and this is defined as.

2. What is a 555 IC?

   The 555 timer IC is a very cheap, popular and useful precision timing device which can act as either a simple timer to generate single pulses or long time delays, or as a relaxation oscillator producing a string of stabilized waveforms of varying duty cycles from 50 to 100%.

3. What are astable, monostable?

   Clock pulse generation circuits can be a combination of analogue and digital circuits that produce a continuous series of pulses (these are called Astable multivibrators) or a pulse of a specific duration (these are called Monostable multivibrators).

4. What are the applications of astable multivibrator?

   Astable multivibrators are used in the applications like pulse position modulation, frequency modulation, etc. as they are simple, reliable and easy to construct. Get electrical articles deliveredinbox every week

Experiment No: 6 **Date:**

Schmitt Trigger Circuits – using IC 741

AIM:

To design the Schmitt Trigger Circuits – using IC 741

APPARATUS REQUIRED:

S. No.	Name of the Apparatus	Range	Quantity
1	Function Generator	3 MHz	1
2	CRO	30 MHz	1
3	Dual Regulated Power Supply	0-30V	1
4	CRO probes	--------	2

COMPONENTS REQUIRED:

S. No.	Name of the Apparatus	Quantity
1	Resistor 1kΩ	2
2	Resistor 100kΩ	1
3	IC-741	1
4	Bread board	1
5	Connecting wires	As required

CIRCUIT DIAGRAM:

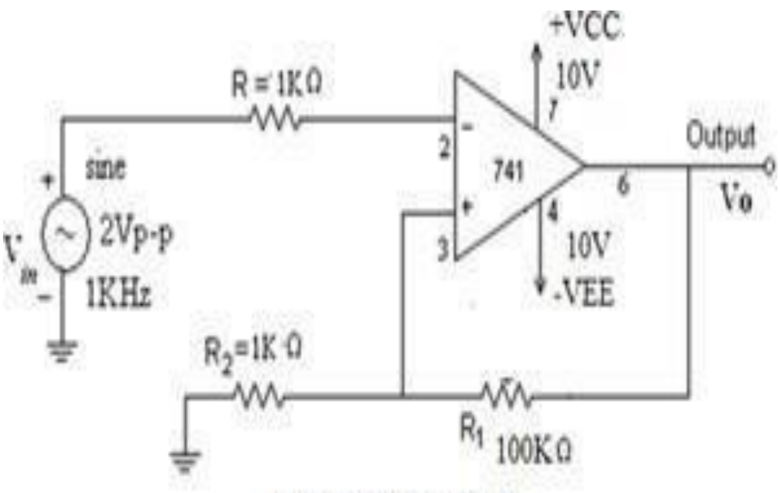


Fig: Schmitt trigger

THEORY:

If positive feedback is added to the comparator circuit, gain can be increased greatly. Regenerative Comparator is also known as Schmitt Trigger .The input voltage is applied to the –ve input terminal and feedback voltage to the +ve input terminal .The input voltage Vi triggers the output Vo every to me it exceeds certain voltage levels. These voltage levels are called upper threshold (V_{UT}) and Lower threshold voltage(V_{LT}).The hysteresis width is the difference between V_{UT} and V_{LT}.

PROCEDURE:

1. Connect the circuit as shown in fig 1(a) as Schmitt trigger using IC 741.
2. Give a 2 Vp-p sine wave of 1 kHz as input.
3. Observe the wave form on CRO and measure UTP and LTP, Vsat and - Vsat.
4. Repeat the above experiment for R1 = 5.1Kohms and 15 K ohms and observe the effect.

OBSERVATIONS:

Peak to peak amplitude of the output=

Upper threshold voltage=

Lower threshold voltage=

PRECAUTIONS:

1. All Connections should be according to circuit diagram.
2. All Connections should be right and tight.
3. Reading should be taken carefully.
4. Switch off Power supply after completing the experiment.
5. Whenever power supply goes automatic switch of all the switch buttons.

EXPECTED WAVE FORMS:

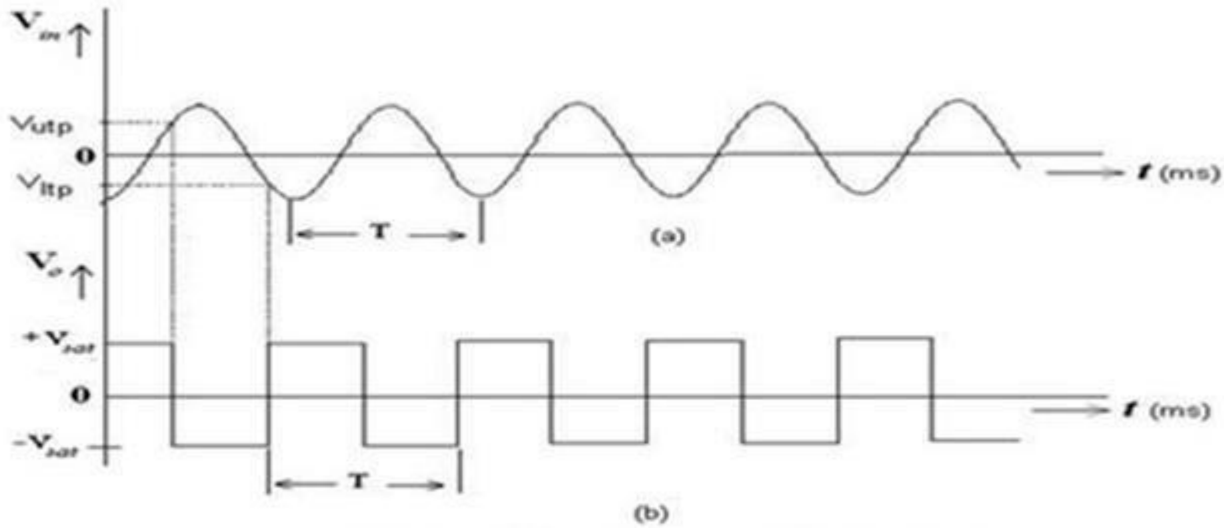


Fig: Schmitt trigger For Input & Output Waveforms

RESULT:

Schmitt trigger designed and studied output waveforms have been drawn.

VIVA QUESTIONS:

1. What is Schmitt Trigger?
   A Schmitt Trigger is a comparator circuit with hysteresis implemented by applying positive feedback to the non inverting input of a comparator or differential amplifier. A Schmitt Trigger uses two input different threshold voltage level to avoid noise in the input

2. What are the applications of Schmitt Trigger?
   Schmitt triggers are mainly used for changing a sine wave to square wave. These are normally utilized in applications like signal conditioning for removing signals noise in digital circuits.

3. Define hysteresis action?
   Hysteresis can be a dynamic lag between an input and an output that disappears if the input is varied more slowly; this is known as rate-dependent hysteresis. However, phenomena such as the magnetic hysteresis loops are mainly rate-independent, which makes a durable memory possible

4. Define UTP?
   The UTP and LTP in Schmitt trigger using op-amp 741 are nothing but UTP stands for upper trigger point, whereas LTP stands for the lower trigger point. Hysteresis can be defined as when the input is higher than a certain chosen threshold (UTP), the output is low.

Experiment No: 7 **Date:**

IC 565 – PLL Applications.

AIM:

i. To study the operation of NE565 PLL
ii. To use NE565 as a multiplier

APPARATUS REQUIRED:

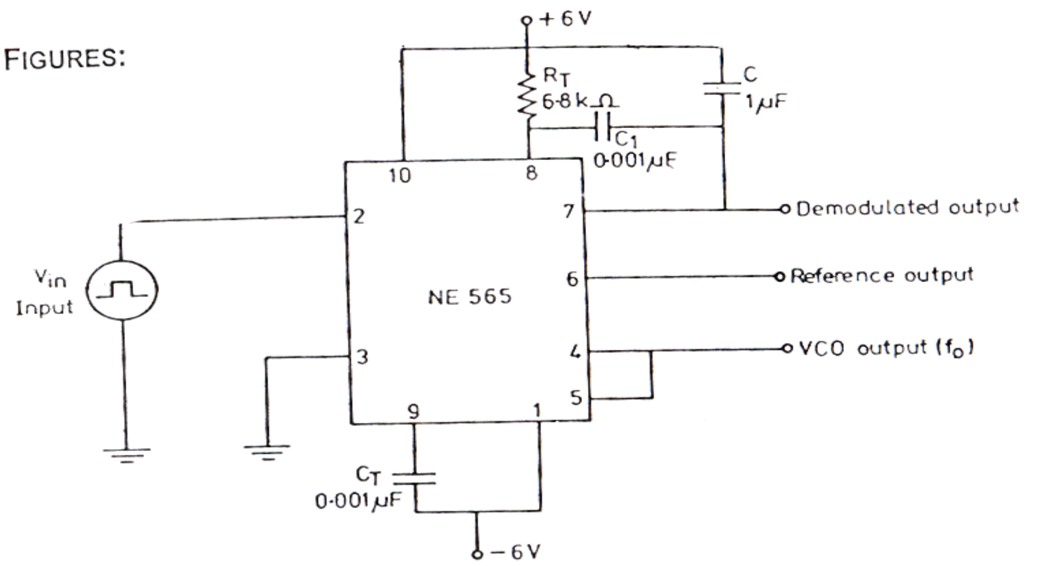
S. No.	Name of the Apparatus	Range	Quantity
1	Function Generator	3 MHz	1
2	CRO	30 MHz	1
3	Dual Regulated Power Supply	0-30V	1
4	CRO probes	--------	2

COMPONENTS REQUIRED:

S. No.	Name of the Apparatus	Quantity
1	Resistors 6.8 kΩ	1
2	Capacitor 0.1µf	1
3	Capacitor 0.001µf	2
4	I.C. 565	1
5	Bread board	1
6	Connecting wires	As required

CIRCUIT DIAGRAM:

FIGURES:

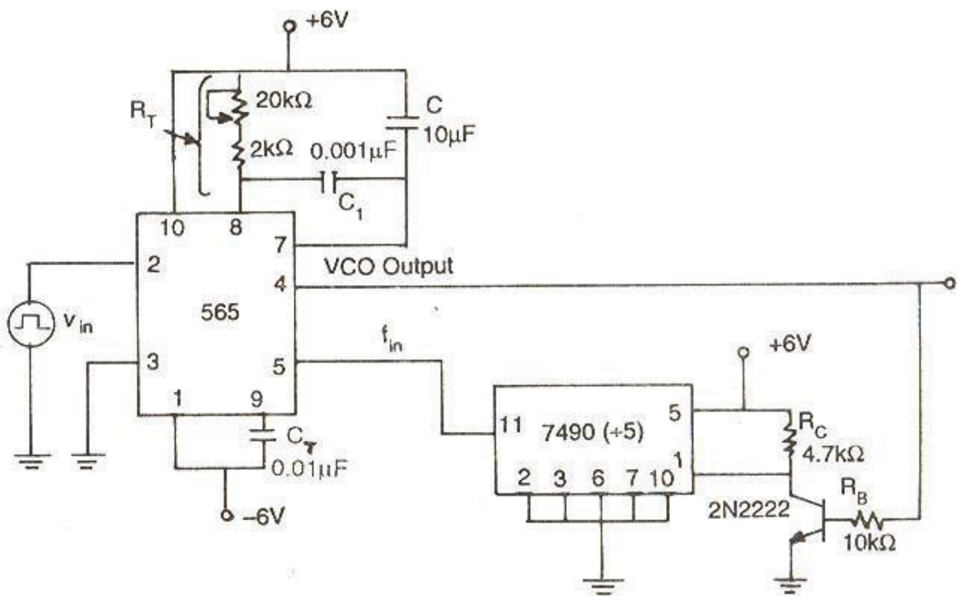


THEORY:

The 565 is available as a 14-pin DIP package. It is produced by signatic corporation. The output frequency of the VCO can be rewritten as

$$f_o = \frac{0.25}{R_T C_T}\ Hz$$

where R_T and C_T are the external resistor and capacitor connected to pin 8 and pin 9. A value between 2 kΩ and 20 kΩ is recommended for R_T. The VCO free running frequency is adjusted with R_T and C_T to be at the centre fo the input frequency range.



PROCEDURE:

iii. Connect the circuit using the component values as shown in the figure

iv. Measure the free running frequency of VCO at pin 4 with the input signal V_{in} set = zero. Compare it with the calculated value = $0.25/R_TC_T$

v. Now apply the input signal of 1Vpp square wave at a 1kHz to pin 2

vi. Connect 1 channel of the scope to pin 2 and display this signal on the scope

vii. Gradually increase the input frequency till the PLL is locked to the input frequency. This frequency $f_1$gives the lower ends of the capture range. Go on increase the input frequency, till PLL tracks the input signal, say to a frequency f_2. This frequency f_2 gives the upper end of the lock range. If the input frequency is increased further the loop will get unlocked.

viii. Now gradually decrease the input frequency till the PLL is again locked. This is the frequency f_3, the upper end of the capture range. Keep on decreasing the input frequency until the loop is unlocked. This frequency f_4 gives the lower end of the lock range

ix. The lock range $\Delta f_L = (f_2 - f_4)$ compare it with the calculated value of $\frac{\pm 7.8 fo}{12}$

Also the capture range is $\Delta f_c = (f_3 - f_1)$. Compare it with the calculated value ofcapture range.

OBSERVATIONS:

fo = ____________

f_L = ____________

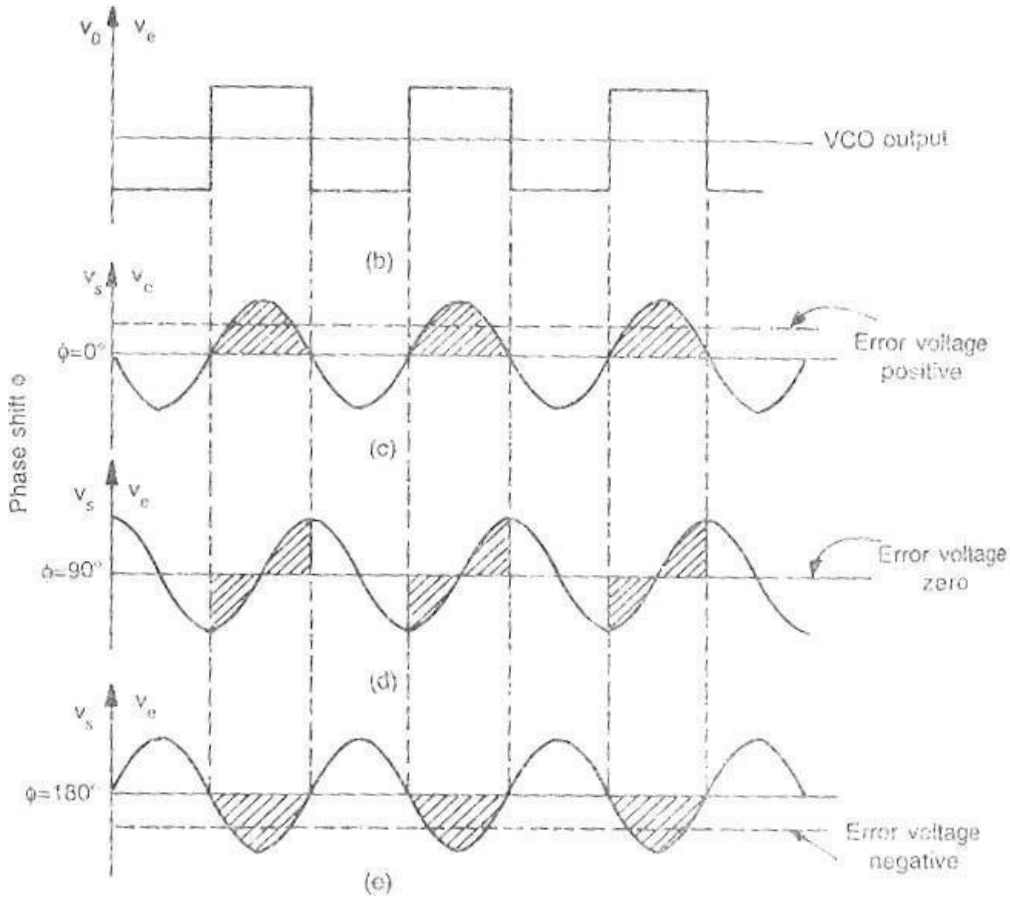
f_C = ____________

CALCULATIONS:

$$\Delta f_L = (f_2 - f_4) = \frac{\pm 7.8 fo}{12}$$

$$\Delta f_c = (f_3 - f_1) = \pm\left[\frac{\Delta f_L}{(2\pi)(3.6)(10^3)xC)}\right]^{1/2}$$

GRAPH:



RESULT:

fo = ___________

f_L =____________ f_C =

____

PRECAUTIONS:

x. Check the circuit connections before switching on the power supply.
xi. Check the connection between pin 7 and 8
xii. Check the connections at the input.
xiii. Check the continuity of the connecting wires.

VIVA QUESTIONS:

1. What are the basic blocks of a PLL?

   The block diagram of a basic PLL is shown in the figure below. It is basically a flip flop consisting of a phase detector, a low pass filter (LPF),and a Voltage Controlled Oscillator (VCO). The input signal Vi with an input frequency fi is passed through a phase detector.

2. Define V_{CO}?

   A voltage-controlled oscillator (VCO) is an electronic oscillator whose output frequency is proportional to its input voltage. An oscillator produces a periodic AC signal, and in VCOs, the oscillation frequency is determined by voltage.

3. What is PLL?

   A phase-locked loop (PLL) is a closed-loop feedback control system, which synchronizes its output signal in frequency as well as in phase with an input signal. The phase detector, the loop filter, and the voltage controlled oscillator are the key parts of almost all PLLs

4. Define lock range?

   The lock range is usually band of frequencies above and below the PLL free running frequency as described earlier. If the frequency of the input signal is outside the PLL lock range than PLL will not be able to lock. Under this condition, VCO frequency jumps to its fundamental free running frequency

5. What are the applications of PLL?

   PLLs are widely used in wireless or radio frequency (RF) applications, including Wi-Fi routers, broadcast radios, walkie-talkie radios, televisions and mobile phones. At its simplest, a phase-locked loop is a closed-loop feedback control circuit that's both frequency- and phase-sensitive.

Experiment No: 8 **Date:**

Voltage Regulator using IC 723, Three Terminal Voltage Regulators – 7805, 7809, 7912.

AIM: To Design a DC power supply using 723, three voltage Regulators-- 7805, 7809.7912

APPARATUS REQUIRED: Regulated DC Power Supply ---------------------------- 1

COMPONTNTS REQUIRED:

S. No.	Name of the Apparatus	Quantity
1	Resistor 10kΩ	1
2	Resistor 100kΩ	1
3	Resistor 560Ω	1
4	Capacitor 100pf	1
5	Decade Resistance Box	1
6	Bread board	1
7	Digital Multimeter	1
8	IC-723	1
9	Connecting wires	As required

THEORY:

We have already explained in detail about the basics of regulated power supply, voltage regulators and IC voltage regulators. Let us take a look at one of the most popular IC voltage regulators, the 723 Voltage Regulator IC. The functional diagram of the voltage regulator is shown below. It consists of a voltage reference source (Pin 6), an error amplifier with its inverting input on pin 4 and non-inverting input on pin 5, a series pass transistor (pins 10 and 11), and a current limiting transistor on pins 2 and 3. The device can be set to work as both posistive and negaive voltage regulators with an output voltage ranging from 2 V to 37 V, and output current levels upto 150 m A. The maximum supply voltage is 40 V, and the line and load regulations are each specified as 0.01%.

We have already explained in detail about the basics of voltage regulators and IC voltage regulators. Let us take a look at one of the most popular IC voltage regulators, the 723 Voltage Regulator IC. The functional diagram of the voltage regulator is shown below. It consists of a voltage reference source (Pin 6), an error amplifier with its inverting input on pin 4 and non-inverting input on pin 5, a series pass transistor (pins 10 and 11), and a current limiting transistor on pins 2 and 3. The device can be set to work as both posistive and negaive voltage regulators with an output voltage ranging from 2 V to 37 V, and output current levels upto 150 m A.

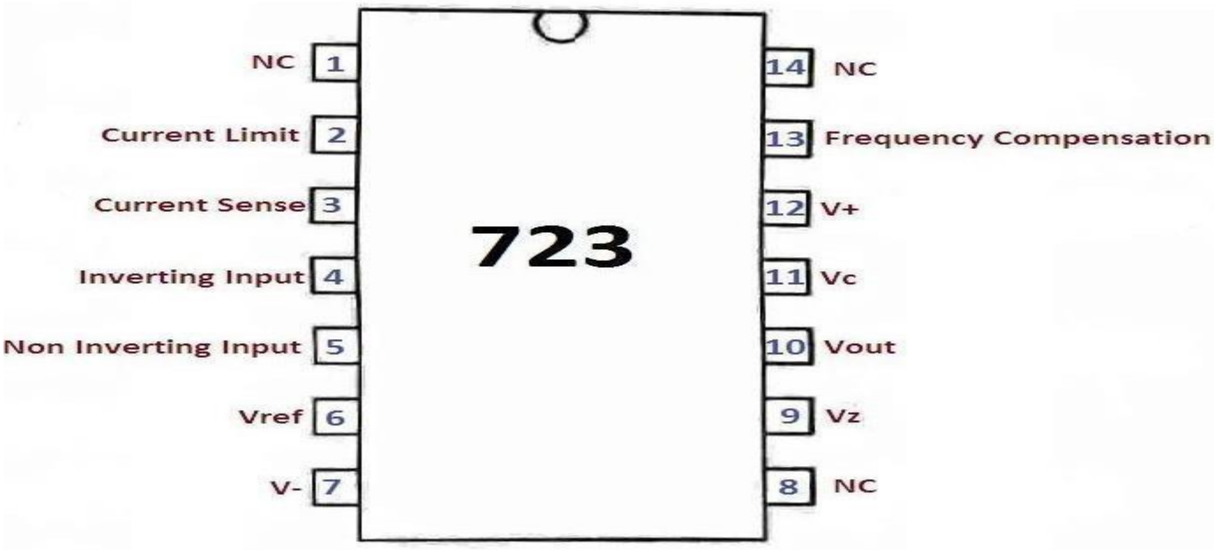


Fig: Pin Diagram of IC-723

CIRCUIT DIAGRAM:

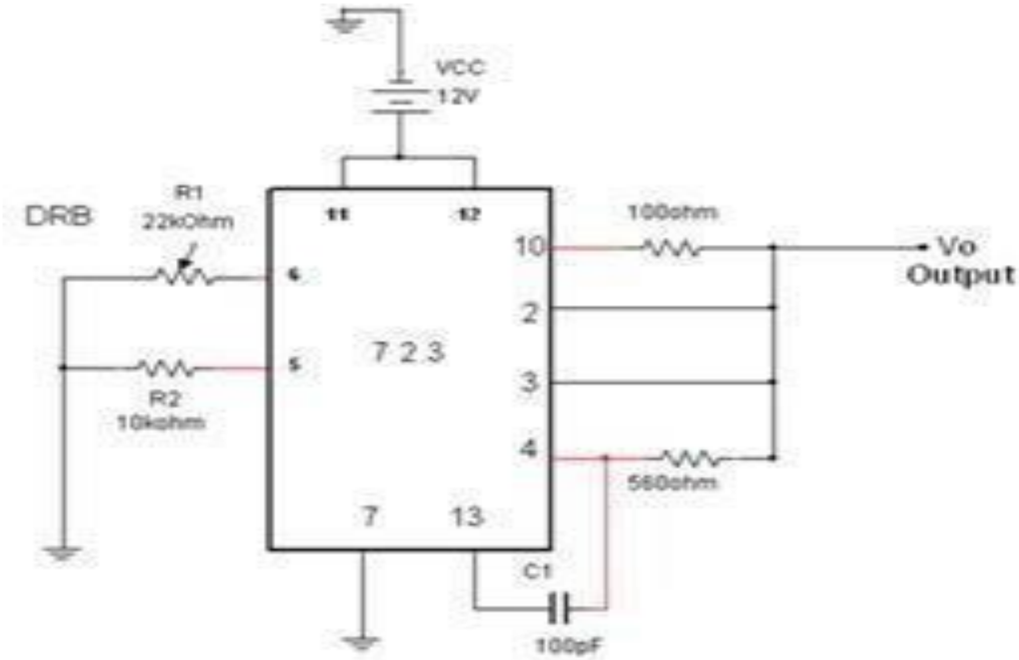


Fig: Low voltage Regulator of IC-723

PROCEDURE:

1) Connect the circuit as per given the circuit diagram.
2) Measure the reference voltage at pin no.6 It should be greater than 7V.
3) By varying the resistance (Decade Resistance Box) measures the output voltage with digital multimeter.
4) Calculate the theoretical values and compare with the practical values.
5) Plot the graph between X-axis on Resistance and Y-axis on Voltage.

EXPECTED WAVE FORMS:

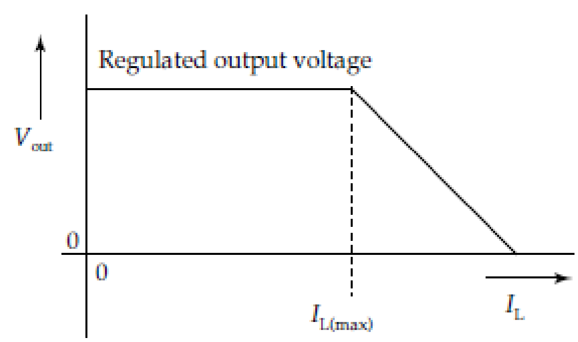


Fig: Output Waveforms For IC-723

TABULAR COLUMN:

SL.NO.	Load Resistance(RL)KΩ	Pin No.6VREF(V)	$V_{OUT} = \left(V_{REF} \times \frac{R2}{R1 + R2}\right)$	Practical V_o(V)
1				
2				
3				
4				
5				
6				
7				

AIM: To study the voltage regulation characteristics and plot the response curve for line regulation and load regulation using 7805, 7809, 7912 ICs.

COMPONTNTS REQUIRED:

S. No.	Name of the Apparatus	Quantity
1	Resistor 10kΩ	1
2	Capacitors 22µF,1000µF	1
3	Ammeter	1
4	Volte meter	1
5	Decade Resistance Box	1
6	Bread board	1
7	Digital Multi meter	1
8	IC-723	1
9	Regulator7805,7905,7912	1
10	Connecting wires	As required

CIRCUIT DIAGRAMS:

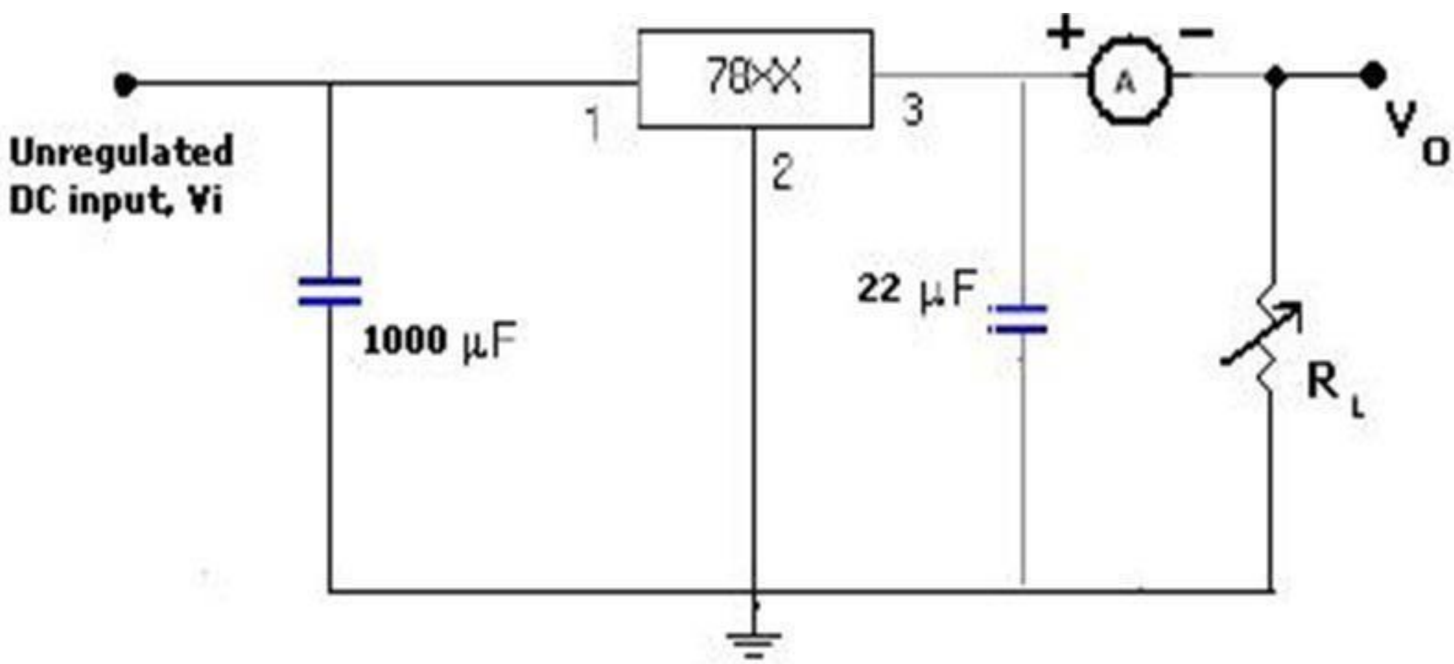


Figure.1 Fixed Positive Voltage regulator

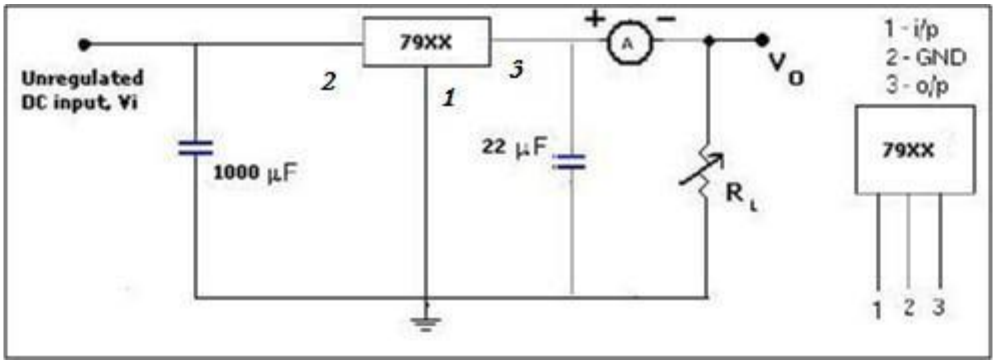


Figure.2 Fixed Negative Voltage Regulator

THEORY: A regulated power supply has to provide constant output voltage irrespective of variation in the load connected to the power supply or variation in the input unregulated power given to the power supply. This is achieved by taking the feedback from the output voltage and compared with a fixed reference voltage. Based on the error, the output voltage is adjusted.

PROCEDURE:

For fixed positive voltage regulator (7805 and 7809):

1. Connect the circuit diagram as shown in figure.1.
2. Apply the unregulated voltage to the IC 7805 and note down the regulator output voltage. Vary input voltage from 7V to 20V and record the output voltages.
3. Calculate the line regulation of the regulator using the formula.
4. Line Regulation = $\Delta V_O / \Delta V_i$.
5. Now, fix the input voltage as 15V and vary the load resistance RL, from 1K to 10 K ohms. Note down the regulator output voltage.
6. Calculate the Load regulation of the regulator using the formula.
7. Load Regulation =$\Delta V_O / \Delta I_L$.
8. Repeat the above procedure for 7809.

For fixed negative voltage regulator (7912):

1. Connect the circuit diagram as shown in figure.2.
2. Apply the unregulated voltage to the IC 7912 and note down the regulator output voltage.
3. Vary input voltage from 7V to 20V and record the output voltages.
4. Calculate the line regulation of the regulator using the formula.
5. Line Regulation = $\Delta V_O / \Delta V_i$.
6. Now, fix the input voltage as 15V and vary the load resistance RL, from 1K to 10 K ohms. Note down the regulator output voltage.
7. Calculate the Load regulation of the regulator using the formula.

OBSERVATIONS:

1). For +Ve Voltage Regulator 7805

Line Regulation: (R_L is constant)

S.No.	Unregulated DC Input, V_i in Volts	Regulated DC Output, V_O in Volts

Load Regulation: (V_i is constant)

S.No.	Load Resistance, R_L in Ohms	Regulated DC output, V_O in Volts

2). For +Ve Voltage Regulator 7809

Line Regulation: (R_L is constant)

S.No.	Unregulated DC Input, V_i in Volts	Regulated DC Output, V_O in Volts

Load Regulation: (V_i is constant)

S.No.	Load Resistance, R_L in Ohms	Regulated DC output, V_O in Volts

3). For -Ve Voltage Regulator 7912

Line Regulation: (R_L is constant)

S.No.	Unregulated DC Input, V_i in Volts	Regulated DC Output, V_O in Volts

Load Regulation: (V_i is constant)

S.No.	Load Resistance, R_L in Ohms	Regulated DC output, V_O in Volts

MODEL GRAPHS (FOR +VE VOLTAGE REGULATORS):

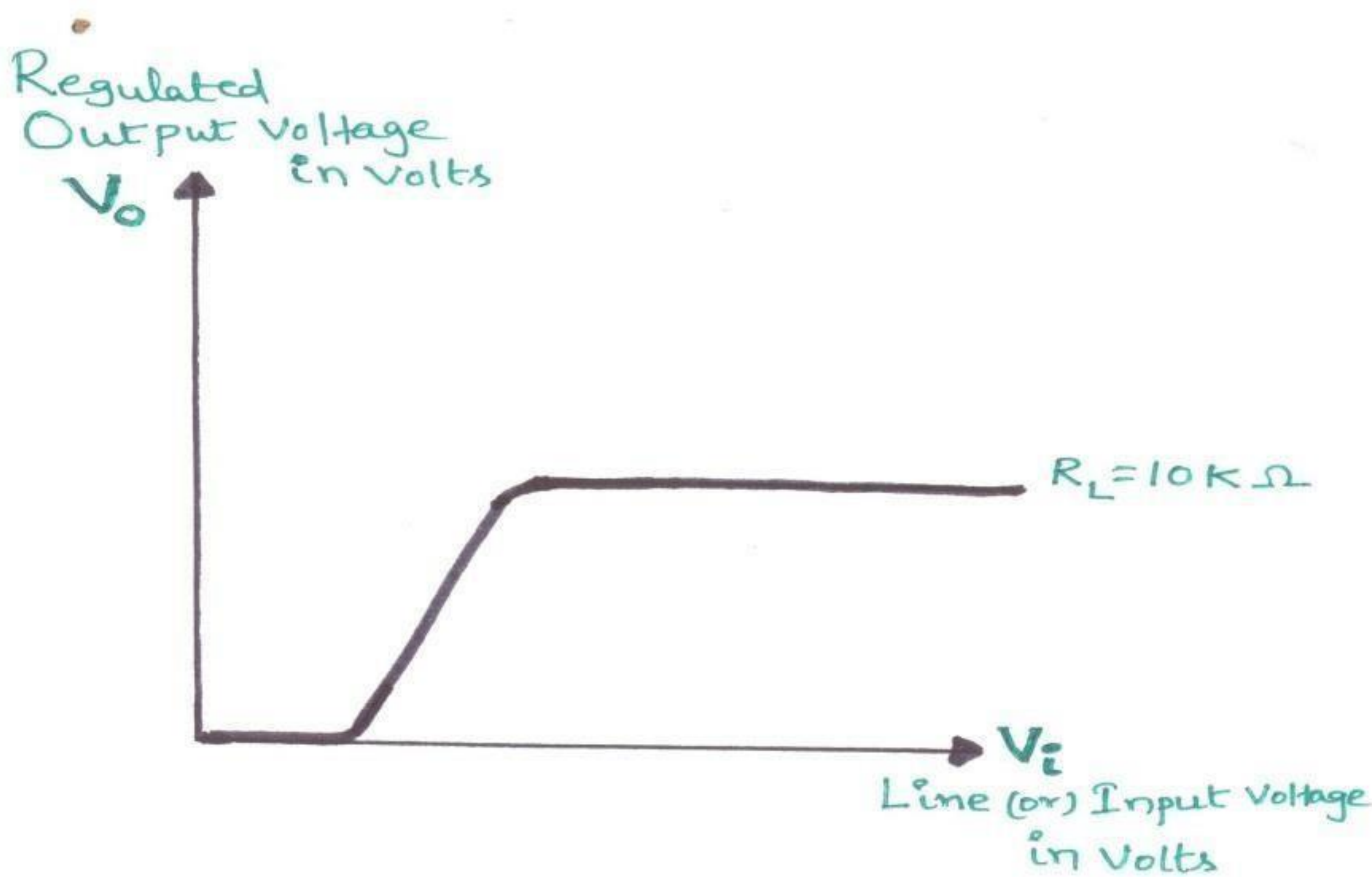


Fig 3. Line Regulation

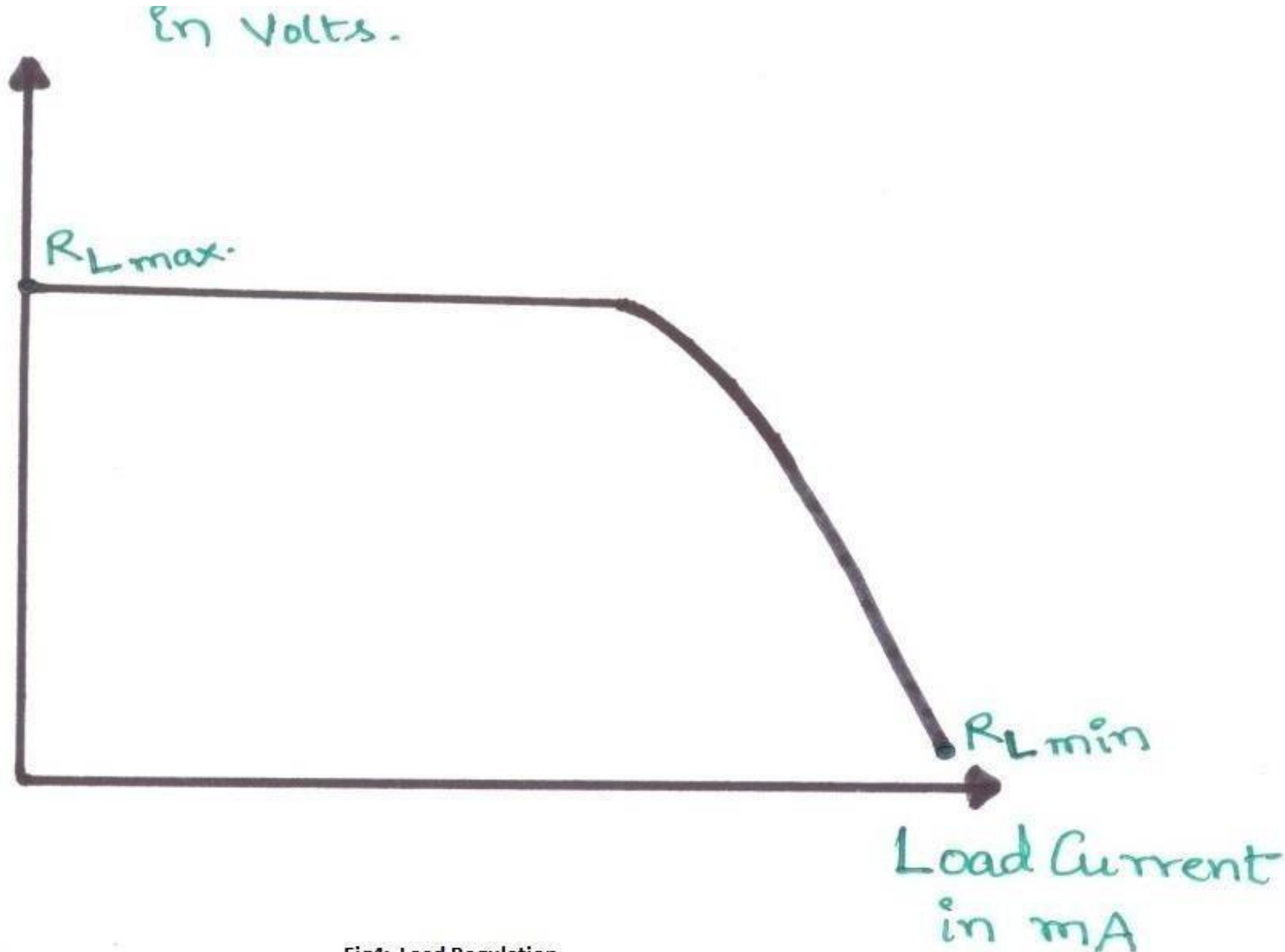


Fig4: Load Regulation

MODEL GRAPHS (FOR -VE VOLTAGE REGULATOR):

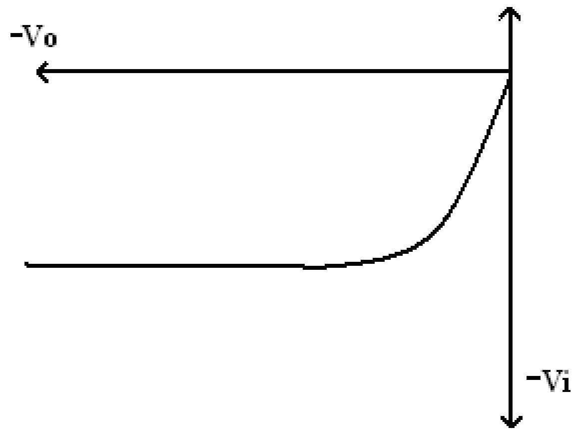


Figure 5. Line Regulation for 79XX

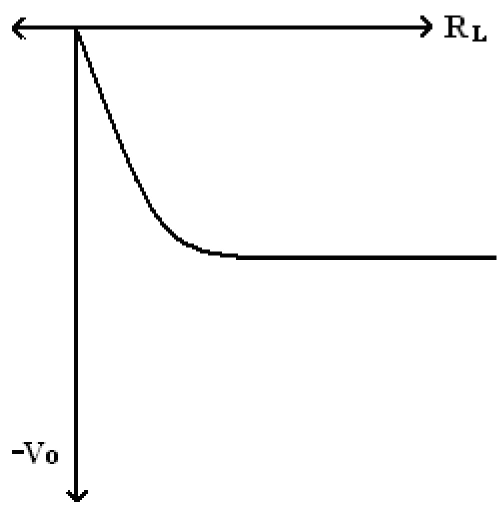


Figure 6. Load Regulation for 79XX

RESULT:

Studied the Voltage Regulator using IC 723, Three Terminal Voltage Regulators – 7805, 7809, 7912 and verified the line & load regulations.

PRECAUTIONS:

1. Do not provide input voltage beyond specified range as with increase in voltage excess electricity is liberated in form of heat from IC 7805 damaging the IC.
2. Use heat sink for input voltages beyond 20-25v
3. Keep current knob of power supply in max position.
4. Check the regulator before connections.
5. Avoid loose contacts.

VIVA QUESTIONS:

1. What is a voltage regulator?

   voltage regulator, any electrical or electronic device that maintains the voltage of a power source within acceptable limits. The voltage regulator is needed to keep voltages within the prescribed range that can be tolerated by the electrical equipment using that voltage

2. How current boosting is achieved in 723 IC?

   The current boosting can be achieved by using external transistor connected in parallel with regulator IC. Thus the output current of 78XX regulator which is 1A can be boosted

3. What is meant by line regulation?

   The ability of a power-supply voltage regulator to maintain its output voltage despite variations in its input voltage.

4. What is meant by load regulation?

   A circuit which is connected between the power source and a load, which provides a constant voltage despite variations in input voltage or output load

PART – II: Digital IC Applications

Experiment No: 1 **Date:**

decoder using 74138

AIM: To verify the functionality of 3-8 Decoder -74LS138 with hardware

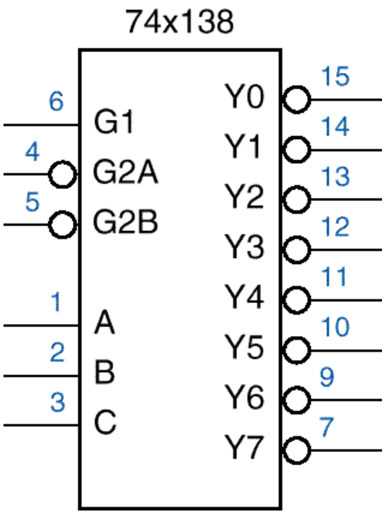
EQUIPMENTS AND COMPONENTS:

1. Digital IC Trainer kit
2. IC 74LS138
3. Regulated Power Supply
4. Connecting wires

THEORY:

A decoder is a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. The 74x138 is a commercially available MSI 3 to 8 decoder. It has an 3-bit binary input code and a 1-out-of-2^3 output code. The input code word A, B, C represents an integer in the range 0 –7, the output code word Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7 which are active low outputs has Yi equal to 1 if and only if the input code word is the binary representation of 'i' and G1 = 1 , G2 A_L = 0, G2 B_L = 0, where G1, G2A_L, G2B_L are three enable inputs. An output is asserted if and only if the decoder is enabled and the output is selected.

PIN CONFIGURATION:



TRUTH TABLE:

PROCEDURE:

2. Connect the circuit as per the pin diagram.
3. Apply the inputs as shown in the truth table and observe the outputs.

OBSERVATIONS: Verify the Truth table

RESULT: The Functionality of 3-to-8 decoder is verified using IC74138.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight on trainer kit.
3. The Vcc and ground should be applied carefully at the specified pin only

VIVA QUESTIONS:

1. What is 3 to 8 decoder why is it used?

   3 to 8 line decoder demultiplexer is a combinational circuit that can be used as both a decoder and a demultiplexer. IC 74HC238 decodes three binary address inputs (A0, A1, A2) into eight outputs (Y0 to Y7). The device also has three Enable pins. The same combination is used as a demultiplexer

2. What can a 3/8 decoder implement?
   3 to 8 line decoder demultiplexer is a combinational circuit that can be used as both a decoder and a demultiplexer. IC 74HC238 decodes three binary address inputs (A0, A1, A2) into eight outputs (Y0 to Y7). The device also has three Enable pins. The same combination is used as a demultiplexer.

3. What are the types of decoder?
   2 to 4 line decoder: In the 2 to 4 line decoder, there is a total of three inputs, i.e., A_0, and A_1 and E and four outputs, i.e., Y_0, Y_1, Y_2, and Y_3. ...
   3 to 8 line decoder: The 3 to 8 line decoder is also known as Binary to Octal Decoder. ...
   4 to 16 line Decoder.

4. What is a decoder used for?
   The name “Decoder” means to translate or decode coded information from one format into another, so a binary decoder transforms “n” binary input signals into an equivalent code using 2^n outputs

Experiment No: 2 **Date:**

4-bit comparator using 7485

AIM: To verify the functionality of 4 bit comparator 74LS85 with hardware

EQUIPMENTS AND COMPONENTS:

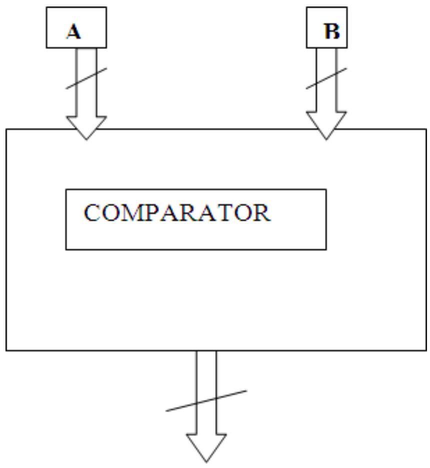
1. Digital IC Trainer kit with IC 74LS85
2. Regulated Power Supply
3. Connecting wires

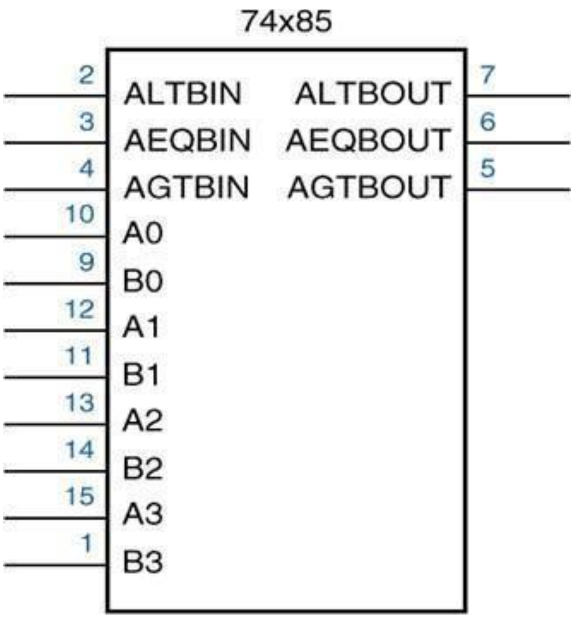
THEORY:

A single bit comparator circuit has 2 data inputs, three control inputs and there compare outputs. The 3 control inputs provide a mechanism for generation of multi bit comparators by cascading several bit comparators.

A 4 bit comparator consists of two 4 bit data inputs 3 control inputs, and 3 compare outputs. The functionality of these circuits is similar to that of the bit comparator. The a>b output is 1 when data on the a input, treated as 4-bit positive number is greater than the 4-bit positive on b or when data on a and b are w\equal and the greater than input is 1. this statement uses a for loop with index I changing from 1 to 2. the outputs are named a_gt_b, a_eq_b, a_lt_b, which are same as primary outputs of a nibble comparator.

HARDWARE IMPLEMENTATION:





TRUTH TABLE:

INPUT A A3 A2 A1 A0	INPUT B B3 B2 B1 B0	ALTBOUT	AGTBOUT	AEQBOUT

PROCEDURE:

1. Connect the circuit as per the pin diagram.
2. Apply the inputs to A and B inputs and observe the outputs.
3. Verify the output with theoretical outputs.

RESULT:

The Functionality of 4-Bit Comparator is verified by IC 74LS85.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight on trainer kit.
3. The Vcc and ground should be applied carefully at the specified pin only

VIVA QUESTIONS:

1. What is the output of a 7485 four bit magnitude comparator?
   C 7485 is a four bit comparator IC. It compares two 4-bit words A(A3−A0) and B(B3–B0). It is possible to cascade mode than one IC 7485 to compare words of almost any length by making use of the cascade pins of the IC.

2. What is a 7485 comparator?
   It compares two 4-bit words A(A3−A0) and B(B3–B0). It is possible to cascade mode than one IC 7485 to compare words of almost any length by making use of the cascade pins of the IC. The logic diagram of IC 7485 is shown below

3. How the comparison of bits takes place in IC 7485?
   There are also discrete ICs available for comparison of binary numbers. In this project SN7485 IC is used which is a 4-bit magnitude comparator. The two 4-bit .

4. How do you create a 4-bit magnitude comparator?
   A comparator used to compare two binary numbers each of four bits is called a 4-bit magnitude comparator.

Experiment No: 3 **Date:**

8*1 Multiplexer using 74151 and 2*4 Demultiplexer using 74155.

AIM:

To verify the functionality of 8 x 1 Multiplexer-74151 and2X4

Demultiplexer – 74155 with hardware

EQUIPMENTS AND COMPONENTS:APPARATUS:

1. Digital IC Trainer kit
2. IC 74LS151, IC 74LS155
3. Regulated Power Supply
4. Connecting wires

THEORY:

IC 74151(MULTIPLEXER)

Multiplexing means transmitting a large number of information units over a smaller number of channels or lines. A digital multiplexer is a combinational circuit that selects binary information from one of many inputs lines and directs it to a single output line. Normally there are 2^n input lines and n selection lines whose bit combinations determine which input is selected. The selection depends onset of selection lines. Also called as selector.

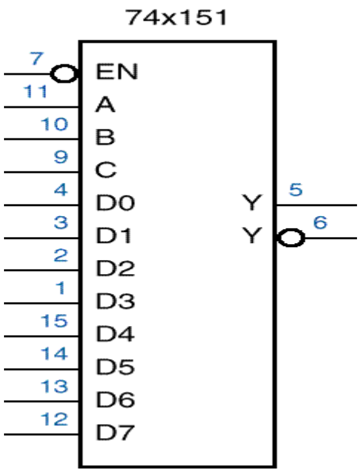
In 8to1 multiplexer, there are 3 select lines and 23 min terms by connecting the function variables directly to select inputs, a multiplexer can be made to a select and AND gate that corresponds to the min terms in the function.

The figure shows an 8-1 multiplexer. It has eight inputs. It provides two outputs, one is active high, and the other is active low.

IC 74155 (2-to-4 LINE DEMULTIPLEXER)

Demultiplexer is a combinational circuit that accepts single input and distributes it several outputs (Selectively distributes it to 1 of N output channels) & Exactly reverse of the multiplexer

PIN CONFIGURATION OF IC 74151:



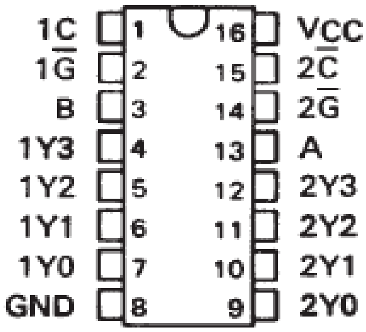
8-GND, 16-VCC

TRUTH TABLE OF IC 74151:

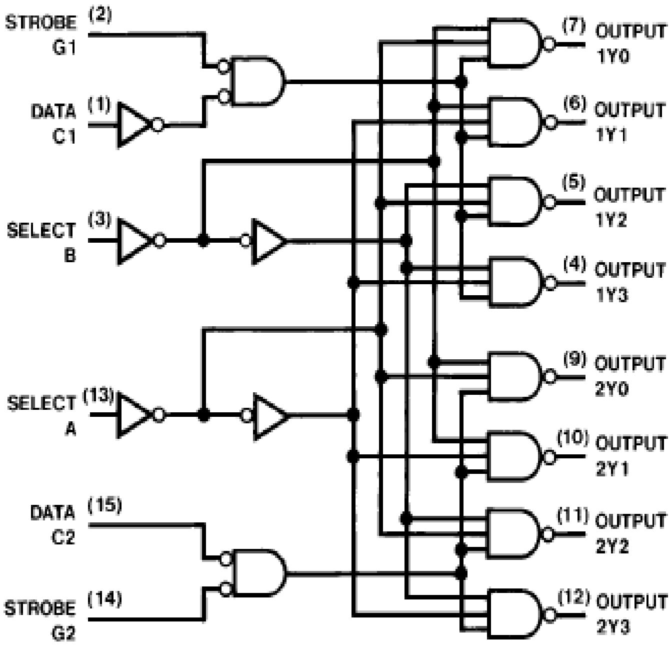
Select i/p				Output
EN_L	**C**	**B**	**A**	**Y**
1	X	X	X	0
0	0	0	0	D_0
0	0	0	1	D_1
0	0	1	0	D_2
0	0	1	1	D_3
0	1	0	0	D_4
0	1	0	1	D_5
0	1	1	0	D_6
0	1	1	1	D_7

.

PIN DIAGRAM OF IC 74155:



LOGIC DIAGRAM OF IC 74155:



TRUTH TABLE OF IC 74155:

INPUTS				OUTPUTS			
SELECT		STROBE	DATA	1Y0	1Y1	1Y2	1Y3
B	A	$1\overline{G}$	1C				
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

PROCEDURE:

1. Connect the circuit as per the pin diagram.
2. Apply the inputs as shown in the truth table and observe the outputs.

RESULT:

The functionality of 8x1 multiplexer and 1x4 line demultiplexer is verified by using ICs.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight on trainer kit.
3. The Vcc and ground should be applied carefully at the specified pin only

VIVA QUESTIONS:

1. What is multiplexer explain 4x1 and 8x1 multiplexers in detail?
   We know that 4x1 Multiplexer has 4 data inputs, 2 selection lines and one output. Whereas, 8x1 Multiplexer has 8 data inputs, 3 selection lines and one output. So, we require two 4x1 Multiplexers in first stage in order to get the 8 data inputs.

2. How many and gates are required for an 8x1 multiplexer?
   In the 8 to 1 multiplexer, there are total **eight inputs**, i.e., A_0, A_1, A_2, A_3, A_4, A_5, A_6, and A_7, 3 selection lines, i.e., S_0, $S_1$and S_2 and single output, i.e., Y. On the basis of the combination of inputs that are present at the selection lines S^0, $S^{1,}$ and S_2, one of these 8 inputs are connected to the output.

3. What is mux and demux and their use?
   A multiplexer (Mux) is a combinational circuit that uses several data inputs to generate a single output. A demultiplexer (Demux) is also a combinational circuit that uses single input that can be

directed throughout several outputs.

4. What is the use of 8x1 multiplexer?
   An 8-to-1 multiplexer consists of eight data inputs D0 through D7, three input select lines S0 through S2 and a single output line Y. Depending on the select lines combinations, multiplexer selects the inputs

Experiment No: 4 **Date:**

D, JK Flip Flops using 7474, 7483.

AIM:

To verify the functionality of D-flip-flop (74LS74) and JK Master-Slave Flip-Flop (74LS73) with Hardware.

EQUIPMENTS AND COMPONENTS:

1. Digital IC Trainer kit
2. IC 74LS74, IC 74LS73
3. Regulated Power Supply
4. Multimeter / Volt Meter
5. Connecting wires.

THEORY:

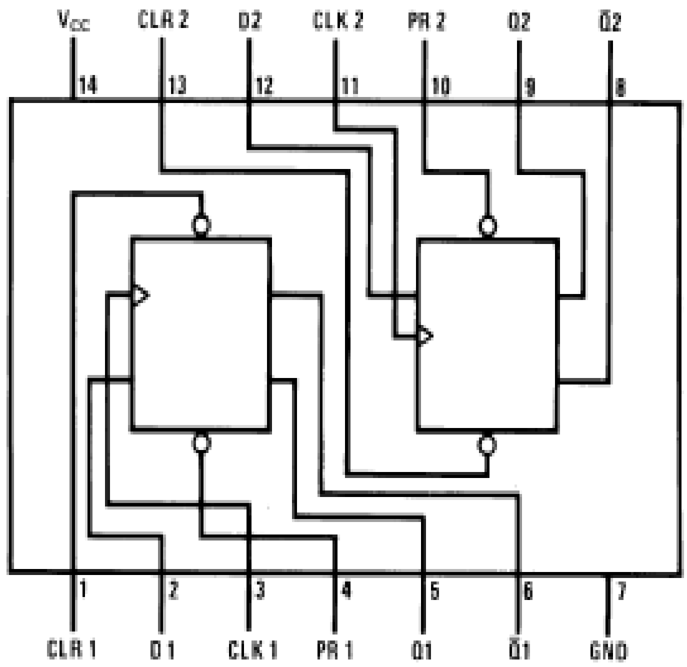
IC 7474

This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

IC 7473

This device contains two independent positive pulse triggered J-K flip- flops with complementary outputs. The J and K data is processed by the flip-flops after a complete clock pulse. While the clock is LOW the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is HIGH the J and K inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic states of the J and K inputs must not be allowed to change while the clock is HIGH. Data transfers to the outputs on the falling edge of the clock pulse. A LOW logic level on the clear input will reset the outputs regardless of the logic states of the other inputs.

PIN DIAGRAM OF IC 74LS74(D FLIP-FLOP):



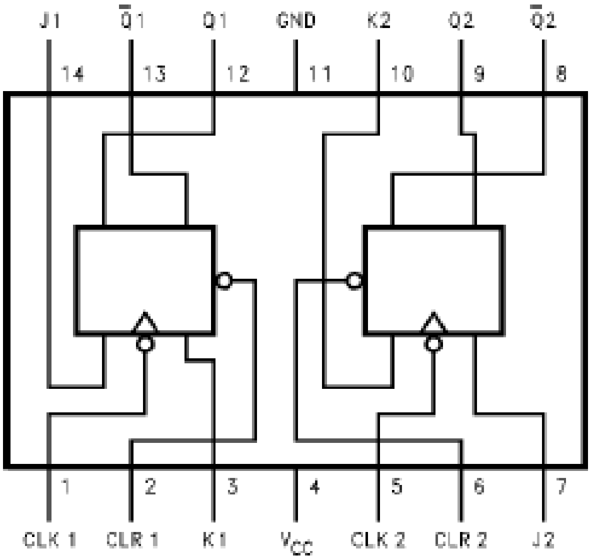
TRUTH TABLE OF IC 74LS74 (D FLIP-FLOP):

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = High Logic Level
X = Either Low or High Logic Level
L = Low Logic Level
↑ = Positive-going transition of the clock.

Note 1: This configuration is non stable ; that is, it will not persist when either the preset and/or clear inputs return to their inactive (high) level. Q0 = The output logic level of Q before the indicated input conditions were established.

PIN DIAGRAM OF IC 7473(MASTER-SLAVE J-K FLIP-FLOP):



TRUTH TABLE:

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\overline{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	Toggle	

H = HIGH Logic Level L =
LOWLogic Level
X = Either LOW or HIGH Logic Level
Q0 = The output logic level before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each HIGH level clock pulse.

PROCEDURE:

2. Connect the circuit as shown in figure.
3. Apply the inputs and verify the truth table of D-flip-flop.
4. Repeat the same for the master-slave JK flip-flop.

TUTORIAL:

1. Realize the D-flip-flop using J-K flip-flop
2. Realize the T-flip-flop from D-flip-flop

RESULT:

The Functionality of D-Flip Flop and master-slave JK flip-flop is verified using ICs.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight on trainer kit.
3. The Vcc and ground should be applied carefully at the specified pin only

VIVA QUESTIONS:

1. Why do the D flip flops is known as data flip flops?
   In D flip flop, the single input "D" is referred to as the "Data" input. When the data input is set to 1, the flip flop would be set, and when it is set to 0, the flip flop would change and become reset.

2. What are JK flip flops used for?
   A J-K flip-flop is nothing more than an S-R flip-flop with an added layer of feedback. This feedback selectively enables one of the two set/reset inputs so that they cannot both carry an active signal to the multivibrator circuit, thus eliminating the invalid condition

3. What is the working principle of JK flip-flop?
   The JK flip flop work as a T-type toggle flip flop when both of its inputs are set to 1. The JK flip flop is an improved clocked SR flip flop. But it still suffers from the "race" problem. This problem occurs when the state of the output Q is changed before the clock input's timing pulse has time to go "Off"..

4. Why JK flip-flop is called universal flip-flop?
   JK Flip Flop is a flip flop which consists of a few logic gates in front of a D-flip flop. A JK flip-flop is also called a universal flip-flop because it can be configured to work as an SR flip-flop, D flip-flop or T flip-flop.

BEYOND THE SYLLABUS EXPERIMENTS

Experiment No: 1 **Date:**

Applications of Op-amp

Design and test the performance of the following circuits using Op-amp IC741/TL082 Inverting amplifier

AIM:

To design and study the open loop gain from Inverting Amplifier circuit.

APPARATUS REQUIRED:

S. No.	Name of the Apparatus	Range	Quantity
1	Function Generator	3 MHz	1
2	CRO	30 MHz	1
3	Dual Regulated Power Supply	0-30V	1
4	CRO probes	--------	2

COMPONENTS REQUIRED:

S. No.	Name of the Apparatus	Quantity
1	Resistor	1.395K
2	Resistor	10.39K
3	Bread board	1
4	IC-741	1
5	Connecting wires	Few No.

SPECIFICATIONS TAKEN:

Inverting Amplifier circuit design has been implemented on the virtual breadboard using following specifications:

· Power Supply: +10v and -10v
· Function generator: Selected wave with following specifications:
 Frequency:1kHz
 Amplitude: 2V
· Resistor R_2: 10.39K

· Resistor R_1: 1.395K

THEORY:

An inverting-amplifier circuit is built by grounding the positive input of the operational amplifier and connecting resistors R1 and R2, called the feedback networks, between the inverting input and the signal source and amplifier output node, respectively. With assumption that reverse-transfer parameter is negligibly small, open-circuit voltage gain Av, input resistance Zin and output resistance Zo can be calculated.

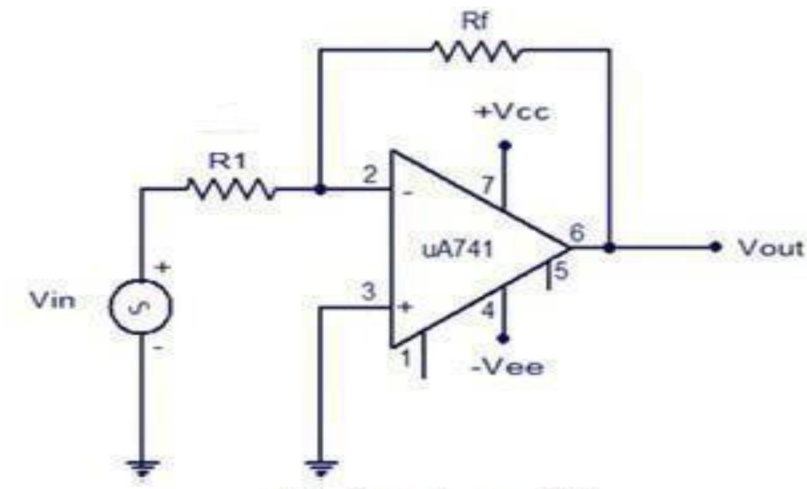


Fig: Inverting amplifier

Inverting Amplifier configuration of an op-amp

PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. Give the input signal as specified.
3. Switch on the power supply.
   Apply a square wave input 2 V_{p-p} and 1 KH_Z to the inverting terminal at pin No.2 using function generator
4. Note down the outputs from the CRO
5. Draw the necessary waveforms on the graph sheet.

OBSERVATIONS:

1. Observe the output waveform from CRO. An inverted and amplified waveform will be observed.
2. Measure the input and output voltage from the input and output waveform in the CRO.
3. calculate

$$V0= -\frac{R_2}{R_1} V_{IN}$$

4. Compare the theoretical voltage gain from the above equation with the experimental value obtained by dividing output voltage by input voltages observed.
5. Observe outputs of the inverting amplifier circuit using different input waveforms.

LAB OBSERVATIONS OBTAINED:

For example, a case has been taken and the required parameters values is being noted down below:

1. Input Voltage: 1.73VV
2. Frequency: 50Hz
3. Output Voltage: 11.9V

CALCULATIONS:

$$A_v = \frac{V_0}{V_{in}} = \frac{11.9V}{1.73V} = 6.88$$

$$A_v = \frac{R_2}{R_1} = \frac{10.39}{1.395} = 7.41$$

1. Theoretically voltage gain is given by:

$$A_v = \frac{R_2}{R_1} = \frac{10.39}{1.395} = 7.41$$

PRACTICAL VALUES:

S. No	R_f	R_1	Input Vp-p	Theoretical input values	Practical output values
1	1K	1K	2.5V	2.5V	2.2V
2	1K	2.2K	2.5V	5.5V	4.4V
3	1K	4.7K	2.5V	11.75V	10V

EXPECTED WAVE FORMS:

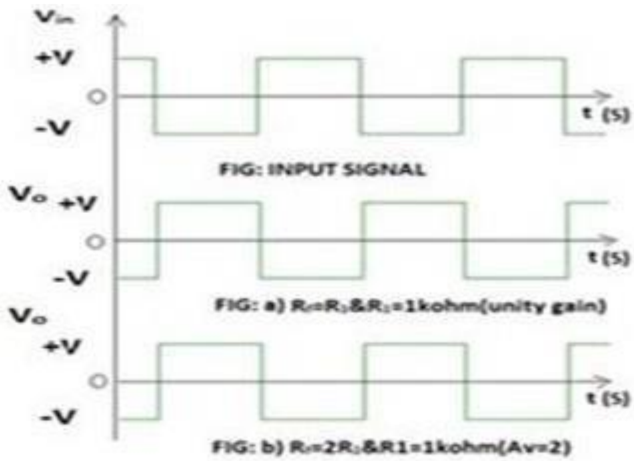


FIG: INVERTING AMPLIFIER

PRECAUTIONS:

1. Connections should be verified before clicking run button.
2. The resistance to be chosen should be in K ohm range.
3. Best performance is being obtained within 50Hz to 1Mhz.

VIVA QUESTIONS:

1. What is an op-amp?

   An operational amplifier (op-amp) is an integrated circuit (IC) that amplifies the difference in voltage between two inputs. It is so named because it can be configured to perform arithmetic operations

2. Adder is used in?

   An op-amp based adder produces an output equal to the sum of the input voltages applied at its inverting terminal. It is also called as a summing amplifier, since the output is an amplified one. In the above circuit, the non-inverting input terminal of the op-amp is connected to ground

3. What is called a Subtractor or differential amplifier?

   A differential amplifier (also known as a difference amplifier or op-amp subtractor) is a type of electronic amplifier that amplifies the difference between two input voltages but suppresses any voltage common to the two inputs

4. What is the purpose of a comparator in op amps?

The Op-amp comparator compares one analogue voltage level with another analogue voltage level, or some preset reference voltage, V_{REF} and produces an output signal based on this voltage comparison

Experiment No: 2 **Date:**

Precision rectifiers

Conduct experiments on half wave and full wave precision rectifiers and draw the output wave forms.

AIM:

To Conduct experiments on half wave and full wave precision rectifiers and draw the output wave forms

EQUIPMENT REQUIRED:

Equipment	Range/Type	Purpose
Dual regulated Power supply	±12V	For biasing the device
Function generator	1 MHz	To provide input
Oscilloscope	20 MHz dual channel	To observe and measure input/output

COMPONENTS REQUIRED:

Component	Specification	Quantity	Purpose
Op-amp	IC741	1	Amplification
Diode	1N4148	2	Rectification
Resistor R1	9.1k	1	input resistor
Resistor R2	9.1 k	1	feedback resistor
Resistor R3	4.7 k	1	Compensation resistor
Resistor R4	1 k□	1	Load

THEORY:

A rectifier is a circuit that converts alternating current (AC) to Direct current (DC). An alternating current always changes its direction over time, but the direct current flows continuously in one direction. In a typical rectifier circuit, we use diodes to rectify AC to DC. But this rectification method can only be used if the input voltage to the circuit is greater than the forward voltage of the diode which is typically 0.7V. We previously explained diode-based half-wave rectifier and full-wave rectifier circuit.

To overcome this issue, the **Precision Rectifier Circuit** was introduced. The precision rectifier is another rectifier that converts AC to DC, but in a precision rectifier we use an op-amp to compensate for the voltage drop across the diode, that is why we are not losing the 0.6V or 0.7V voltage drop across the diode, also the circuit can be constructed to have some gain at the output of the amplifier as well

So, in this tutorial, I am going to show you how you can **build, test, apply, and debug a precision rectifier circuit using op-amp**. Alongside that, I will be discussing some pros and cons of this circuit as well. So, without further ado, let's get started. The above figure shows the characteristics of an **ideal rectifier circuit** with its transfer characteristics. This implies when the input signal is negative, the output will be zero volts and when the input signal is positive the output will follow the input signal.

CIRCUIT DIAGRAM:

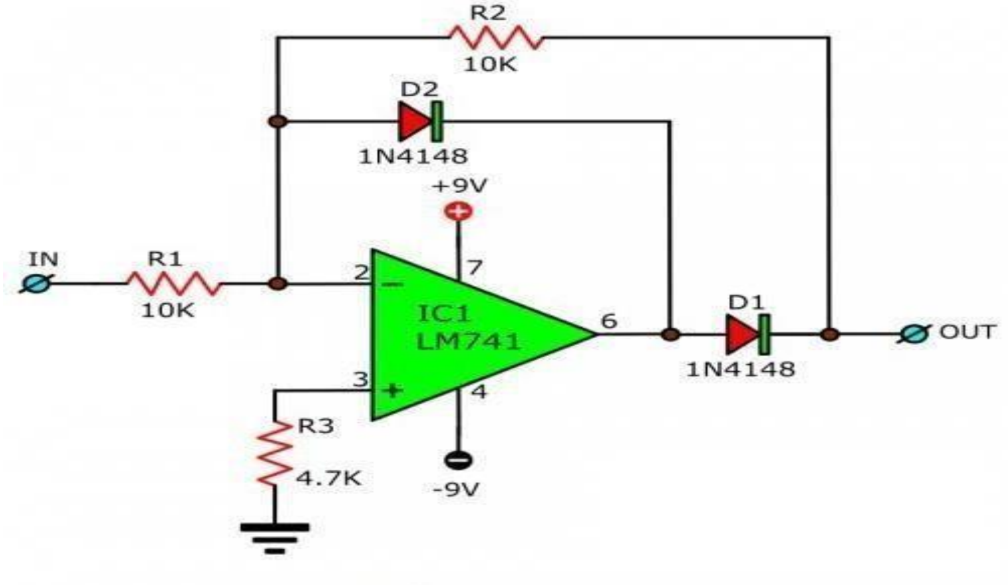


Fig: Half wave precision rectifier

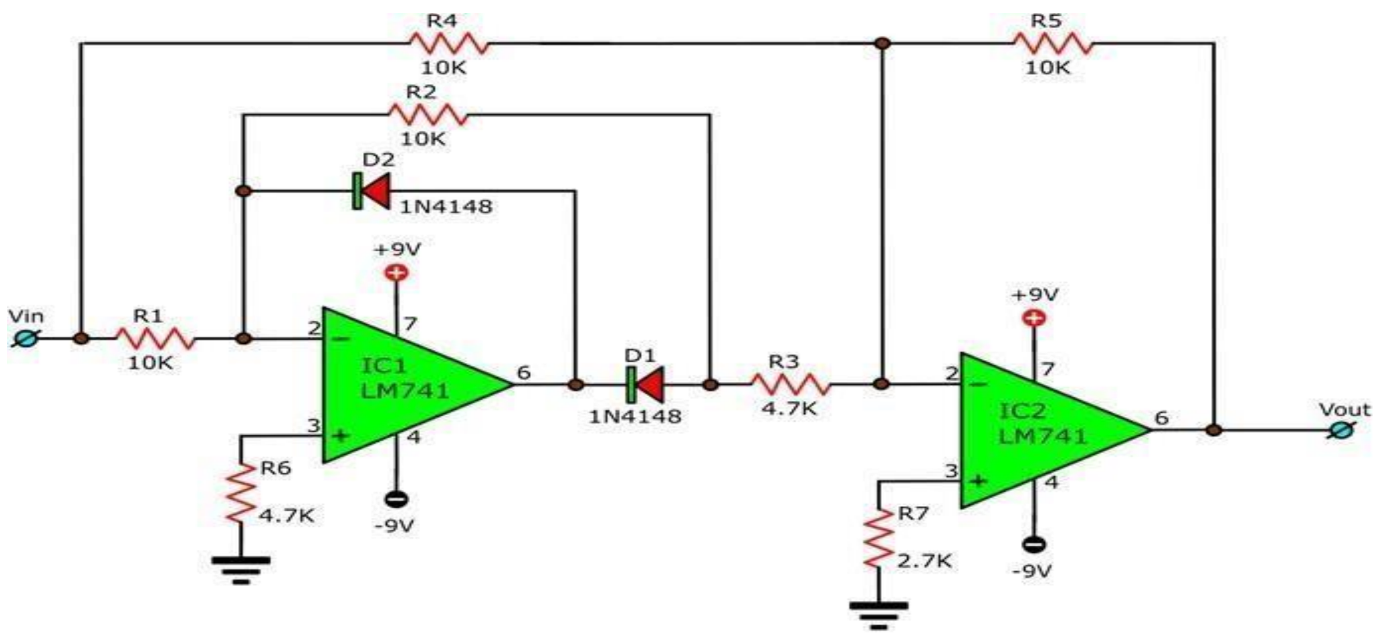


Fig: Full wave precision rectifier

PROCEDURE:

1) Connect the circuit as per the circuit diagram.
2) The bias voltages are applied to the circuit i.e. 4^{th} and 7^{th} pin numbers.
3) Using function generator, adjust the amplifier of input sinusoidal voltage to $2V_{P-P}$ and 1khz freq.
4) Precision half-wave rectifiers are commonly used with other op amp circuits such as a peak-detector or bandwidth limited non-inverting amplifier to produce a DC output voltage.
5) This configuration has been designed to work for sinusoidal input signals between 0.2mVpp and 4Vpp at frequencies up to 50kHz

EXPECTED WAVE FORMS:

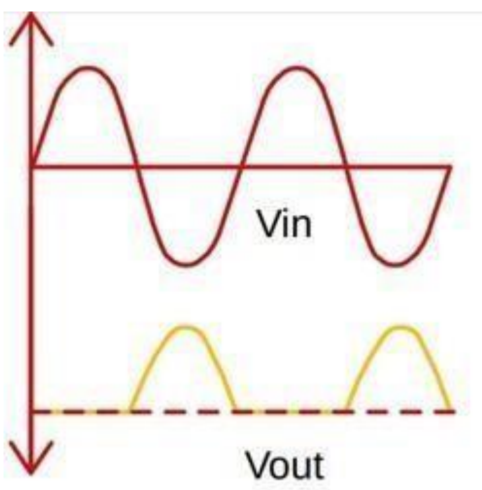


Fig: Half wave precision rectifier

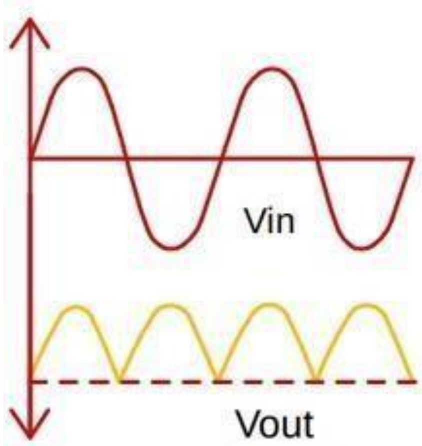


Fig: Full wave precision rectifier

PRACTICAL VALUES:

Half wave rectifier:

Amplitude: 2x0.5=1v

Time period: 10x0.5ms=0.5ms

Full wave rectifier:

Amplitude: 2x5=10v

Time period:

2x0.5ms=1msRESULT:

We have designed and studied the Precision rectifiers using half wave and full wave with 741 IC, we have drawn the output waveforms.

VIVA QUESTIONS:

Half wave rectifier:

1. Explain why half-wave rectifiers are generally not used in dc power supply**?**

Ans. The type of supply available from half-wave rectifier is not satisfactory for general power supply. That is Explain why it is generally not used in dc power supply.

2. Discuss in detail about different types of rectifiers and its features?

Ans. There are mainly 3 different types of rectifiers namely: Half wave, full wave and Bridge rectifiers. Out of these three, Bridge rectifier is the best one among these because Bridge rectifier has more efficiency, less ripple factor, more TUF, less peak factor, less PIV and less transformer cost.

3. Explain the process of converting AC to DC?

Ans.The process of converting an AC voltage to DC voltage requires 4 steps. First the AC voltage is fed to a step down transformer. The 230V, 50Hz input AC voltage is step down to 10-30 V AC voltage. This reduced voltage passes through a rectifier circuit. The heart of a rectifier circuit is a diode. After the rectifier, the voltage is passed to filter circuit. Capacitor is the base of a filter circuit.

4. Explain in detail about regulation and the need of regulation?

Ans.Basically we can say that regulation is the measure of change in the magnitude between the sending and receiving end of a component. The use of a voltage regulator is to keep the power level in a stabilized manner. The main use of voltage regulation is to keep the voltages within the required range of a electrical equipment. In other words, in order to keep an electrical equipment work in its prescribed voltage levels, regulation circuit is used.

Full wave rectifier:

1. Explain why diodes are not operated in the breakdown region in rectifiers?

Ans. In breakdown region, a diode has a risk of getting damaged or burnt because the magnitude of current flowing through it increases in an uncontrollable manner. That is Explain why diodes are not operated in the breakdown region in rectifiers.

2. Define ripple as referred to in a rectifier circuit.

   Ans. The ac component contained in the pulsating output of a rectifier is known as ripple.

. 3. The output of a 60Hz full-wave bridge rectifier has a 60 Hz ripple. It this circuit working properly?

Ans. A full-wave rectifier with 60Hz input must have lowest ripple frequency equal to twice the input frequency i.e. 120Hz. If the ripple frequency is 60Hz, it means some diodes in the circuit are not working.